# Design of mmWave Power Amplifier for Base Station Application in 5G

*Dissertation submitted to*
*Visvesvaraya National Institute of Technology, Nagpur*
*in partial fulfillment of the requirements for the award of*
*the degree*

**Master of Technology in**

**Communication System Engineering**

**by**

**Garima Gattani (MT23CMN004)**

under the guidance of

**Prof. Abhay Gandhi**

**Department of Electronics and Communication**

**Visvesvaraya National Institute of Technology**

**Nagpur 440 010 (India)**

**June 2025**

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**Department of Electronics and Communication Engineering**

**Visvesvaraya National Institute of Technology, Nagpur**

## DECLARATION

I, **Garima Gattani**, hereby declare that this dissertation titled **"*Design of mmWave Power Amplifier for Base Station Application in 5G*"** is carried out by me in the **Department of Electronics and Communication Engineering** of Visvesvaraya National Institute of Technology, Nagpur. The work is original and has not been submitted earlier whole or in part for the award of any degree/diploma at this or any other Institution / University.

**Garima Gattani**

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## CERTIFICATE

This is to certify that the dissertation titled **"*Design of mmWave Power Amplifier for Base Station Application in 5G*"** is submitted by **Garima Gattani (MT23CMN004)** in partial fulfillment of the requirements for the award of **Master of Technology in Communication System Engineering**, VNIT Nagpur. The work is comprehensive, complete, and fit for final evaluation.

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Professor, Electronics and
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Communication Engineering
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# Non-Plagiarism Certificate

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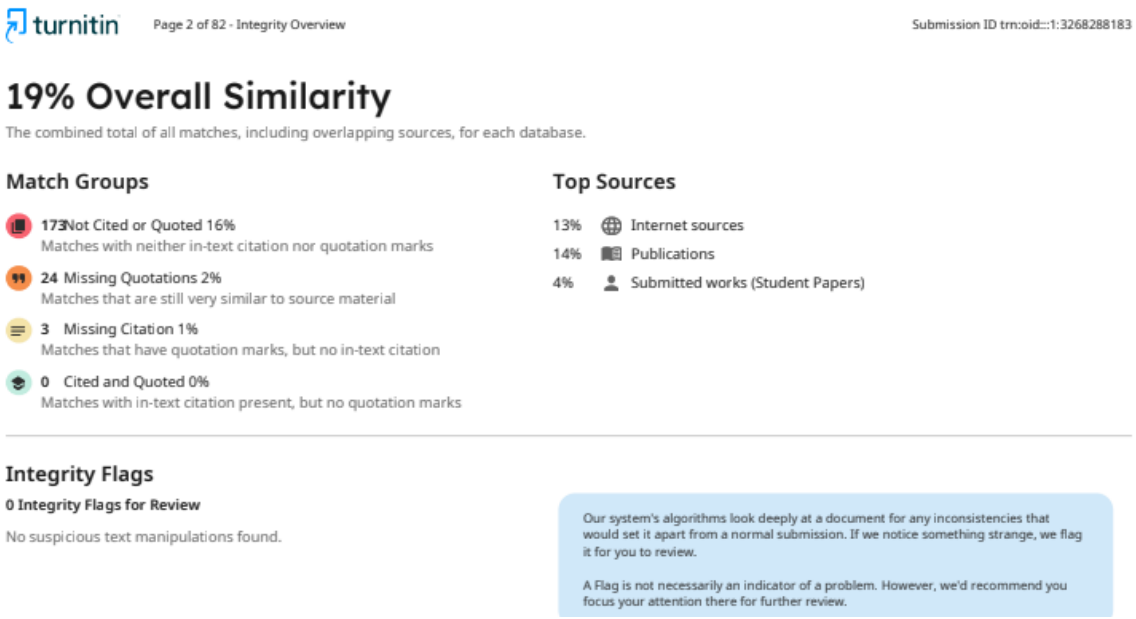
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Their guidance and support played a crucial role in helping me bring this work to fruition.

**Garima Gattani**

**MT23CMN004**

# ABSTRACT

The evolution of fifth-generation (5G) wireless networks demands power amplifiers (PAs) capable of operating efficiently at millimeter-wave (mmWave) frequencies, particularly in the 25–30 GHz band allocated for 5G base stations. Due to high path loss in this range, the PA plays a critical role in the radio frequency (RF) front-end by boosting signal strength, maintaining linearity, and minimizing power consumption. This project presents the design and evaluation of a broadband PA based on GaN-on-Si ASM-HEMT technology, which is well-suited for high-frequency, high-power applications due to its high breakdown voltage, electron mobility, and thermal robustness.

The designed PA targets the 25–30 GHz bandwidth and delivers a peak gain of 15 dB at 28 GHz, aligning with the center of the targeted 5G band. It maintains strong performance across the band, with Power-Added Efficiency (PAE) ranging from 55% at 25 GHz to 45% at 30 GHz, meeting the efficiency requirements for continuous operation under high peak-to-average power ratios. Input matching is optimized, with the reflection coefficient $|S_{11}|$ showing a magnitude of 0.267 at 28 GHz, corresponding to a return loss of 11.5 dB, indicating minimal signal reflection and good input impedance matching.

The amplifier's characteristics make it highly suitable for 5G base station applications, particularly in phased-array architectures, where wide bandwidth, high gain, and efficient power performance are critical. The use of GaN ASM-HEMT technology ensures that the design meets the thermal and linearity demands of next-generation wireless infrastructure.

**Keywords:** 5G mmWave Power Amplifier,ASM-HEMT Technology, Broadband 25–30 GHz Operation, High Power-Added Efficiency (PAE), Input Matching and Return Loss,

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# Chapter 1

# Introduction

## 1.1 Overview of Wireless Communication Spectrum

### 1.1.1 Global Spectrum Utilization

- **North America (U.S./Canada):** Utilizes bands such as 600 MHz, 700 MHz, and 850 MHz for FDD, with additional bands like 2300 MHz and 2600 MHz supporting both FDD and TDD operations.
- **Europe:** Adopts bands including 450 MHz, 800 MHz, and 900 MHz for FDD, and 2600 MHz for TDD, balancing coverage and capacity.
- **China and Southeast Asia:** Focus on bands such as 900 MHz and 1800 MHz for FDD, with 2300 MHz and 2600 MHz deployed for high-capacity TDD services.
- **Japan and South Korea:** Feature a similar mix, with added usage of 2500 MHz and 3500 MHz for advanced services.
- **India and MENA (Middle East and North Africa):** Utilize bands like 850 MHz, 1800 MHz for FDD and 2300 MHz, 2600 MHz for TDD services.
- **Australia and Latin America:** Follow similar allocation patterns, supporting both low-band and mid-band deployments for broad coverage and enhanced capacity.

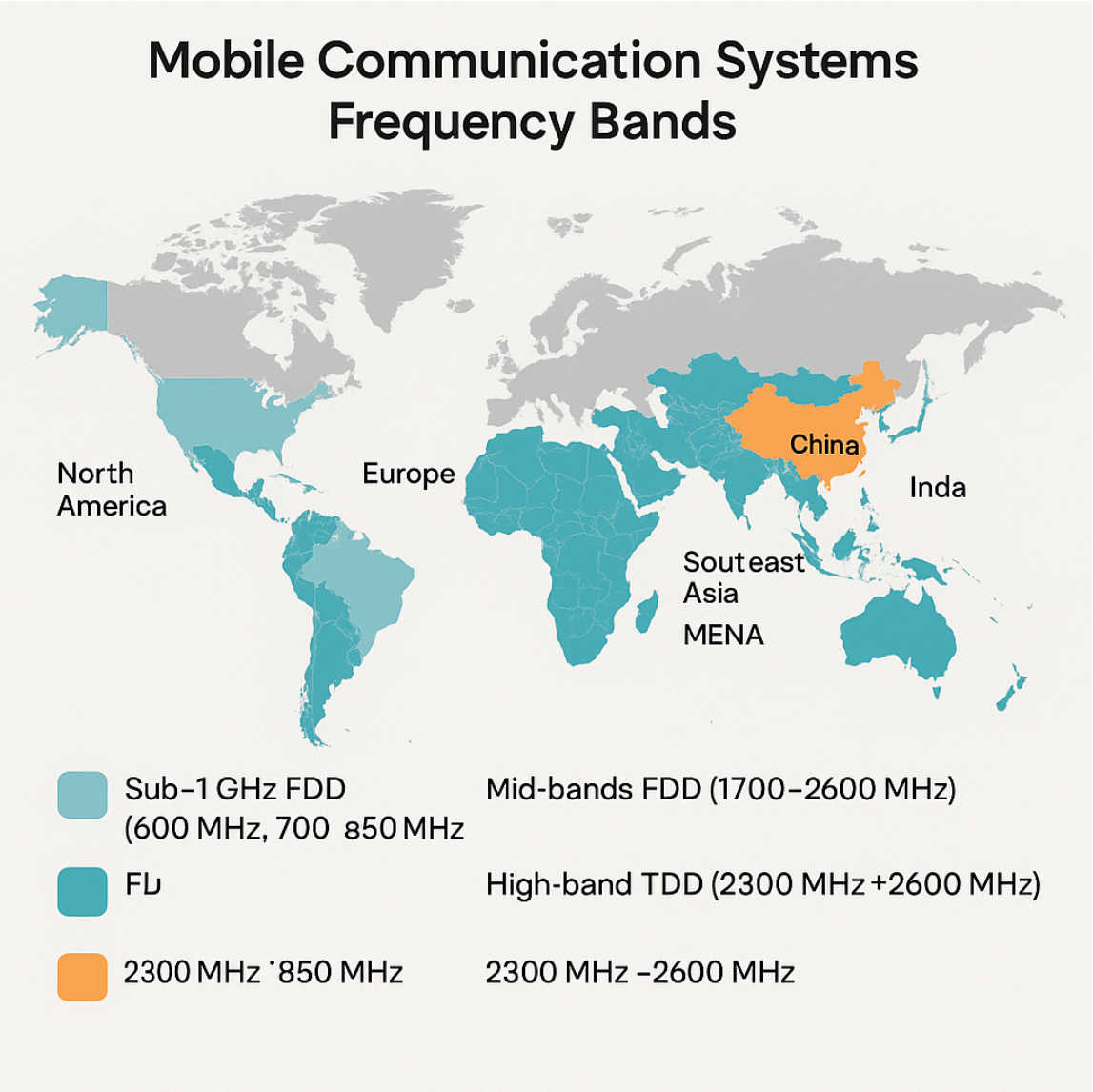


**Figure 1.1: Global frequency allocation of mobile communication bands including FDD and TDD technologies across various regions. [1]**

### 1.1.2 Key Observations

- Low-frequency bands (<1 GHz) are widely deployed for broader coverage and deep indoor penetration due to favorable propagation characteristics.
- Mid-bands (1.7–2.6 GHz) are used for a balance of capacity and coverage, forming the backbone of many 4G LTE and early 5G deployments.
- High-band TDD allocations (e.g., 2300 MHz, 2600 MHz) are extensively utilized in urban and dense environments to meet high data traffic demands.
- The global diversity in spectrum usage highlights the complexity in designing power amplifiers (PAs) and RF front-end modules, which must support multiple bands and duplexing modes to enable seamless global roaming and device interoperability.

## 1.2 Motivation for 5G mmWave PA Development

Wireless communication technology is moving toward fifth-generation (5G) Advanced and sixth-generation (6G) systems to satisfy the rapidly growing needs for increased data rates and network capacity. Power amplifiers (PAs), which continue to be the most power-intensive parts of the transceiver chain and have a major impact on the system's overall output power, power consumption, and linearity, are subject to more stringent performance criteria as a result of this evolution.

The Shannon-Hartley theorem states that the channel capacity is directly proportional to the channel bandwidth (BW), which is the theoretical maximum data throughput possible at a given signal-to-noise ratio (SNR). To take advantage of much wider bandwidths available at mmWave frequencies, 5G communications are gradually moving from the sub-6 GHz (FR1) bands to mmWave frequency range 2 (FR2) bands and beyond, where spectrum bands such as 26–30 GHz are targeted.

## 1.3 Challenges in mmWave PA Design

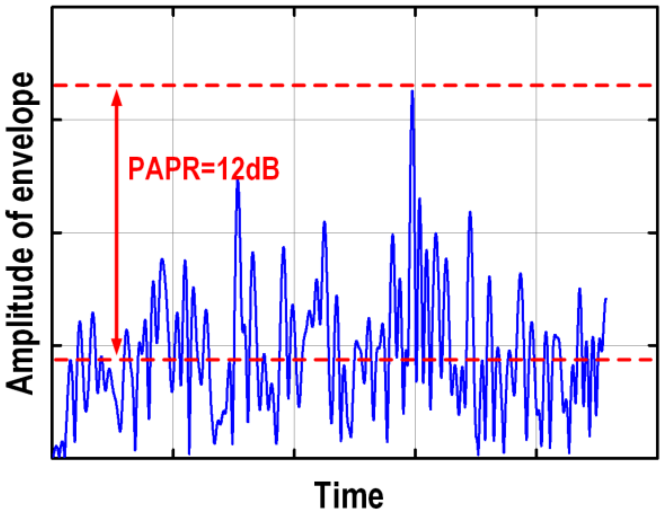


**Figure 1.2: Time-domain envelope of a typical OFDM modulated signal exhibiting a peak-to-average power ratio (PAPR) of 12 dB. [2]**

At mmWave frequencies, achieving high-efficiency and high-linearity performance becomes increasingly challenging due to:

- Higher free-space path loss and atmospheric absorption, requiring higher PA output power and beamforming.
- The use of high-order modulation schemes (e.g., 64-QAM, 256-QAM) that require the PA to operate efficiently at significant power back-off (PBO) due to large PAPR waveforms like OFDM.
- There is a critical need for wide instantaneous bandwidths ($\geq 1\,\text{GHz}$) to effectively support the 5G New Radio (NR) Frequency Range 2 (FR2) bands, such as n257 and n258, which operate in the millimeter-wave spectrum.
- Integration with phased arrays and beamforming front-ends in compact form factors, demanding minimal parasitics and broadband impedance matching.

These challenges necessitate innovative PA architectures and design techniques to meet the stringent requirements of 5G mmWave systems operating in the 26–30 GHz band.

## 1.4 Problem Statement

The deployment of 5G base stations in the millimeter-wave spectrum, particularly in the 25–30 GHz range, necessitates the development of power amplifiers that are efficient, broadband, and capable of delivering high linear output power under challenging conditions. Traditional PA topologies often suffer from poor back-off efficiency, narrow bandwidth, and high power dissipation when operating at such high frequencies.

The primary objective of this work is to design and implement a high-efficiency mmWave PA optimized for 5G base station applications in the 25–30 GHz frequency range. The proposed design aims to address key performance challenges, including:

- Maintaining high power-added efficiency (PAE) across a wide bandwidth.
- Achieving good linearity and spectral purity under high peak-to-average power ratio (PAPR) conditions.
- Ensuring compatibility with phased-array front-end architectures.
- Minimizing die area, matching losses, and thermal dissipation.

To meet these goals, this work will explore suitable PA classes—such as Class AB, Class J, or other advanced switching-mode architectures—and optimize them for broadband operation and high efficiency in the targeted frequency band.

# Chapter 2

# Literature Review

- Design of 5GHz Class-J Power Amplifier using Silterra 0.13 µm CMOS Technology

  Tuffy et al.[4] presented a Class-J RF power amplifier design operating at 5 GHz using the Silterra 0.13 µm CMOS technology, targeting high-efficiency performance suitable for 5G wireless applications. The study focuses on leveraging the inherent benefits of Class-J operation, particularly its capability to achieve high power-added efficiency (PAE) over a wide bandwidth without compromising linearity.

  To handle the limitations posed by the low breakdown voltage in CMOS processes, the authors implemented a stacked transistor architecture, which allows higher output voltage swing. Harmonic tuning is accomplished through a parallel RLC circuit, enabling effective waveform shaping necessary for Class-J operation. Additionally, the design incorporates optimized input and output matching networks to maximize gain and power transfer.

  The simulation results demonstrate an output power of 17.6 dBm, a power-added efficiency (PAE) of 44.5%, and a power gain of 16.1 dB at 5 GHz. These performance metrics confirm the amplifier's suitability for modern communication systems, particularly in the context of 5G standards where both efficiency and linearity are critical.

  This work validates the feasibility of implementing efficient and compact Class-J

power amplifiers in standard CMOS technology, making it a promising candidate for integration in low-cost, high-frequency RF front-ends.

- A 27 GHz, 14 dBm CMOS Power Amplifier Using 0.18 μm Common-Source MOSFETs

  Lee and Heo (2008) [5] present a Ka-band three-stage CMOS power amplifier designed using 0.18 μm gate-length common-source transistors. The amplifier targets applications in high-frequency short-range communications such as automotive radar and 60 GHz WPAN systems, where compact, low-cost, and efficient RF front-ends are essential.

  The design leverages substrate-shielded microstrip lines to minimize insertion loss and improve matching accuracy up to 40 GHz. On-wafer measurements revealed an insertion loss of 0.5 dB/mm at 25 GHz. The amplifier stages utilize common-source transistors rather than the more common cascode configuration, aiming for higher efficiency and better compatibility with low-voltage deep sub-micron CMOS technologies.

  A hybrid matching approach combining distributed and lumped elements was employed, and the amplifier was biased at a low voltage to maintain high power efficiency. The fabricated chip, measuring only 0.84 $mm^2$, demonstrated a small-signal gain of 14.5 dB, saturated output power of 14 dBm, and a power-added efficiency (PAE) of 13.2% at 27 GHz. These performance metrics represent some of the best reported results for CMOS PAs using common-source topology in the Ka-band.

  The study highlights that common-source configurations, when carefully optimized, can achieve high gain and efficiency at mmWave frequencies, offering a viable alternative to cascode topologies for compact and power-efficient CMOS RF designs.

- A Highly Linear and Efficient 28-GHz PA in 65-nm Bulk CMOS

  Asoodeh et al.[6] present a 28-GHz power amplifier (PA) implemented in 65-nm bulk CMOS, targeting high linearity and efficiency for 5G applications. The proposed PA

achieves a saturated output power ($P_{sat}$) of 23.2 dBm, 1-dB compression point ($P_{1dB}$) of 22.7 dBm, and peak power-added efficiency (PAE) of 35.5%.

The PA employs a two-stage architecture with a linearity enhancement technique that utilizes a varactor-controlled adaptive feedback network. This network dynamically adjusts the impedance seen by the output transistor based on output power, effectively minimizing both AM–AM and AM–PM distortions. A CPW-like output combiner and a source-inductance cancellation network are used to improve passive efficiency and gain stability.

Measurement results confirm excellent performance with an error vector magnitude (EVM) of –26.2 dB and adjacent channel power ratio (ACPR) of –28.3 dBc for 64-QAM signals at 2.5 GS/s. The PA demonstrates high efficiency and linearity over a wide frequency range (26–31 GHz), validating its suitability for phased-array 5G transceivers.

This work highlights the effectiveness of combining analog feedback and EM-optimized passive structures to achieve competitive performance in standard bulk CMOS for mm-wave PAs.

- Design of a Broadband High-Efficiency Hybrid Class-EFJ Power Amplifier

  Zhiwei Zhang et al.[7] introduce a novel hybrid power amplifier (PA) topology, referred to as Class-EFJ, which combines the high-efficiency characteristics of Class-EF PAs with the broadband capabilities of Class-J PAs. The objective is to overcome the narrow bandwidth limitations of traditional high-efficiency amplifiers while maintaining competitive drain efficiency.

  Theoretical analysis is provided to establish the compatibility of Class-EF and Class-J load impedance conditions. Based on this, a Class-EFJ PA is designed using the CGH40010F GaN HEMT on a Rogers 4350B substrate. Harmonic control circuits are implemented to ensure ideal conditions: the second harmonic is shorted while the third harmonic is open, using carefully designed microstrip transmission lines.

The fabricated PA demonstrates a saturated output power between 40.5–42.7 dBm across a wide 1.2–3.6 GHz frequency range. The measured drain efficiency ranges from 63% to 73% across this band. When driven by a 5-MHz W-CDMA signal with a 6.5 dB peak-to-average ratio, the amplifier maintains an average output power of 35.6 dBm with an ACLR better than –31.2 dBc, confirming its linearity under modulated signals.

This work effectively shows that the Class-EFJ architecture achieves a strong balance between bandwidth and efficiency, making it highly suitable for broadband and high-efficiency RF applications.

- Highly Efficient 24-GHz CMOS Linear Power Amplifier with an Adaptive Bias Circuit

  Hyunji Koo et al. present [8] a 24 GHz power amplifier (PA) implemented using a 0.13 μm CMOS process that employs an adaptive-bias circuit to improve power efficiency and linearity. The PA is designed to address the inherent trade-offs in CMOS PAs between idle power efficiency and output power by dynamically adjusting the gate bias based on input power.

  The amplifier comprises a two-stage architecture: a cascode driver stage and a common-source power stage. The adaptive-bias circuit operates in a differential configuration and generates gate voltages that increase with input power, resulting in a steeper gain near the 1-dB compression point (P1dB). This technique improves both output power and power-added efficiency (PAE) without the need for external control circuitry.

  The fabricated chip, occupying an area of 0.5 $mm^2$, demonstrates a measured output P1dB of 13.3 dBm and a PAE of 15.6% at P1dB. Compared to a fixed-gate-bias PA, the adaptive-bias approach improves output power by 1.2 dB and PAE by 4%, while maintaining similar quiescent power consumption. The maximum saturated output power reaches 16 dBm with a peak PAE of 17.7%.

This work shows that adaptive biasing in CMOS PAs can effectively enhance efficiency at back-off power levels, making it suitable for low-voltage, high-frequency applications such as 24 GHz wireless transceivers.

- Doherty Power Amplifier Design Based on Joint Adaptive Adjustment of Bias and Input Power

  Wei Xue et al.[9] propose an enhanced Doherty Power Amplifier (DPA) architecture that integrates joint adaptive adjustment of gate bias, drain bias, and input power allocation to improve output power back-off (OPBO) and overall power-added efficiency (PAE). The design specifically addresses the degradation in DPA efficiency under high peak-to-average power ratio (PAPR) signals due to the knee-voltage effect.

  In the conventional DPA, performance is limited by static biasing and symmetric input power distribution, which lead to early saturation and reduced efficiency at back-off levels. In this work, the authors introduce a dynamic control scheme wherein:

  – The gate and drain bias of both the Carrier and Peaking amplifiers are adaptively modulated.

  – The input power is asymmetrically split between the branches, allowing for more optimal drive conditions.

  Three configurations were tested: (A) fixed-bias DPA, (B) adaptive bias DPA, and (C) adaptive bias with controlled input power splitting. Experimental results using Cree GaN HEMT CG2H40010F at 3.5 GHz demonstrate:

  – OPBO extension from 5 dB to 7 dB,

  – A maximum output power of 44.4 dBm,

  – An average efficiency improvement of 3% with adaptive input power allocation.

  This method significantly enhances DPA performance under high PAPR signals by ensuring efficient power utilization across output power levels. It offers a promising approach for linear and efficient PAs in modern wireless systems.

- Neural Network Based GaN HEMT Modelling for Millimeter Wave Power Amplifiers

  Kenya Nishiguchi [10] et al. present a novel large-signal modeling approach for GaN High Electron Mobility Transistors (HEMTs) targeting millimeter-wave power amplifiers using artificial neural networks (ANN). The model uniquely applies the ANN only to the nonlinear current source component of a compact model, addressing challenges such as short-channel effects and data overfitting, which are prevalent in millimeter-wave device modeling.

  To train the ANN model, pulsed I–V and S-parameter measurements were conducted up to 120 GHz. Small-signal parasitics, including resistances and inductances, were extracted near the load-line using a conventional equivalent circuit and represented through nonlinear functions, while the capacitances were modeled with hyperbolic tangent functions to avoid the noise sensitivity of raw measurements.

  The ANN architecture employed three hidden layers with sigmoid activation functions, and optimization was carried out using the ADAM algorithm. Simulation results demonstrated that the ANN model accurately captured key nonlinear behaviors, including current collapse and short-channel effects, which were not effectively modeled by traditional compact models.

  The model was verified by implementing it in Verilog-A and integrating it within an RF circuit simulator. A fabricated amplifier operating at 71 GHz validated the model's accuracy through comparison with measured DC, small-signal, and large-signal performance. The ANN-based model showed strong agreement with measured data across varying impedance conditions, confirming its robustness.

- A 24–29 GHz GaN Power Amplifier for Monolithic Millimeter-Wave RF Front-End

  This work presents[11] a broadband power amplifier (PA) monolithic microwave integrated circuit (MMIC) operating in the 24–29 GHz frequency band, fabricated using a 0.1 $\mu$m GaN-on-Si process. The design is motivated by the growing demand for high-efficiency, wideband millimeter-wave (mmWave) PAs suitable for RF front-

ends in next-generation wireless communication systems.

The PA employs a three-stage cascade topology with device periphery ratios of 1:2:4, ensuring adequate gain and saturated output power. A moderate transistor size of $8 \times 50\,\mu$m was chosen to achieve a balanced trade-off between broadband impedance matching and output power capability. To address the gain roll-off issue at higher frequencies, the design integrates a second-order low-pass matching network along with an RLC-based gain compensation circuit to enhance gain at lower frequencies.

Ensuring stability is a critical concern in single-sided power supply architectures. To address this, the design incorporates low-frequency RC parallel networks at the gate terminals of the transistors, series RC filtering in the bias paths, high-frequency decoupling capacitors, and isolation resistors in the final stage. These techniques successfully suppress low-frequency and odd-mode oscillations, resulting in unconditional stability over the 0–100 GHz frequency range.

The simulationation results show a saturated output power exceeding 34.7 dBpower added efficiency (PAE) greater thangreater than 31%, and a flat gain greater than 21 dB across the 24–29 GHz band. The input and output return losses are better than –12 dB and –14 dB, respectively, indicating excellent impedance matching across the band. The compact die layout, measuring $3 \times 1.4\,\text{mm}^2$, is optimized for symmetry and testability.

Overall, the proposed GaN MMIC PA demonstrates high power, efficiency, and stability, establishing its suitability for integration into broadband mmWave RF front-end modules intended for future communication systems.

- Class J Power Amplifier for 5G Applications in 28 nm CMOS FD-SOI Technology

  In the paper by Tony Hanna [12], Nathalie Deltimple, and Sébastien Frégonèse , the authors present a Class J power amplifier (PA) designed in 28 nm FD-SOI CMOS technology, targeting sub-6 GHz 5G applications. The motivation stems from the demand for highly efficient and broadband RF PAs for 5G, where Class J offers

superior power-added efficiency (PAE) over a wide bandwidth without the need for complex harmonic terminations. Leveraging the unique properties of FD–SOI —- such as reduced parasitics and body biasing —-the authors implement a single NMOS Class J topology operating at 2.4 GHz. The design features a tuned load network that shapes the fundamental and second harmonic voltage waveforms. Measurement results show an output power of +15.7 dBm, PAE of 38.5%, gain of 15.5 dB, and operation at a 1.2 V supply. This work is significant because it demonstrates the first Class J PA in FD-SOI for 5G use and validates the potential of FD-SOI for efficient RF power amplifier design. It provides a foundational reference for this thesis, which focuses on extending Class J PA design to the Ka-band for 5G user equipment.

- Millimeter-Wave Analog Pre-distorted Power Amplifier at 65nm Node This work by Nasir A. Quadir et al [13] presents the design of a 28 GHz power amplifier (PA) implemented in GlobalFoundries 65 nm CMOS technology, targeting millimeter-wave 5G applications. The PA incorporates a built-in passive analog pre-distortion linearizer based on a cold mode MOSFET to improve linearity and gain expansion at high frequencies. The design uses a two-stage common-source amplifier topology with inductive peaking to maximize gain and employs efficient biasing networks to minimize power consumption. Simulations of the post-layout design demonstrate a maximum small-signal gain of 21.1 dB, an output referred 1-dB compression point (P1dB) of 19.84 dBm, and a power-added efficiency (PAE) of 15%, with an output power reaching 22.4 dBm. The linearizer effectively enhances the PA's linearity and maintains performance across temperature variations from -40°C to 125°C. By using off-chip lumped elements for impedance matching, the design optimizes chip size and tuning flexibility. Compared to previous works, this PA achieves superior linear output power and gain with a smaller technology node, making it a promising solution for high-frequency 5G power amplification.

- GaN HEMTs for 5G base station applications This article by Shigeru Nakajima [14] presents the development and advantages of Gallium Nitride High Electron Mobility

Transistors (GaN HEMTs) on SiC substrates for 5G base station applications. GaN HEMTs have been commercially available since 2005 and offer several benefits over traditional silicon-based technologies.

- **Material Superiority:** GaN on SiC offers high breakdown voltage, high electron mobility, and low resistance to the infrared, resulting in higher power efficiency and broader frequency response. The thermal conductivity of the SiC substratetrate (3x that of Si) enhances heat dissipation, enabling reliable high-power operation.
- **Performance:** GaN HEMTs achieve:
  - Inverse Class F operation: saturated power 50 dBm, drain efficiency 70% at 2.14 GHz.
  - Sub-6 GHz Doherty amplifiers:
    - C-plane: 56 dBm Psat, 52.2% efficiency at 7 dB back-off.
    - U-plane M-MIMO: $>$ 47 dBm output power, $>$ 60% peak efficiency, $>$ 45% at 8 dB back-off over 4.35–4.85 GHz.
  - mmWave ($>$ 20 GHz) Doherty MMIC: 26 dBm Pout, $>$13% PAE, 16 dB gain with 7% bandwidth.
- **Reliability:** Achieved MTTF $> 10^7$ hours at $T_j = 200°C$. Over 20 million units shipped with field failure rate $<$1 FIT. The robustness of the device is ensured through quality control of the SiC substrates, epitaxial layers, and electrode fabrication.
- **Cost Reduction:** Cost optimization was achieved through the use of large-diameter substrates, low-cost and non-hermetic packaging, and development of moisture-resistant chips meeting JEDEC standards.
- **Relevance to 5G:** GaN HEMTs are highly suited for 5G base stations requiring high efficiency, wide bandwidth, and compact form factors. Devices with $f_T$

and $f_{max} > 100$ GHz support operation $> 10$ Gbps, meeting the 5G mmWave demands.

**Conclusion:** GaN HEMTs are proven, reliable, and efficient solutions for current and future 5G base station amplifier designs, supporting both sub-6 GHz and mmWave bands.

# Chapter 3

# Methodology , Tools and Technology used

## 3.1 Tools Used

The Cadence AWR Design Environment Platform streamlines the development of RF and microwave products by automating design processes, increasing engineering efficiency, and shortening development cycles. This unified platform provides powerful high-frequency circuit and system simulation, along with integrated electromagnetic (EM) and thermal analysis capabilities, enabling the creation of manufacturing-ready, high-performance RF IP with exceptional accuracy and speed.

## 3.2 Overview of the Cadence AWR Design Environment

The **Cadence AWR Design Environment** is a powerful, integrated electronic design automation (EDA) platform specifically tailored for the development of RF, microwave, and millimeter-wave circuits and systems. Widely used in both academia and industry, AWR provides a streamlined workflow for the design, simulation, and optimization of high-frequency components such as power amplifiers, LNAs, mixers, oscillators, and full transceiver chains.

### 3.2.1 Key Features

- **Unified Simulation Environment:** Combines circuit, system, and electromagnetic (EM) simulation within a single interface, reducing design iteration cycles and improving productivity.
- **High-Frequency Circuit Simulation:** Supports linear and nonlinear analyses such as S-parameter, harmonic balance, load-pull, noise, and stability simulations.
- **EM Co-Simulation:** Integrates with planar EM solver AXIEM and full 3D solver Analyst for layout-aware and full-wave EM modeling of passive structures and packages.
- **System-Level Design:** Offers VSS (Visual System Simulator) for end-to-end simulation of RF transmit/receive chains, including behavioral models and modulation schemes.
- **Technology Compatibility:** Supports foundry process design kits (PDKs) and a wide range of compact models such as BSIM3, BSIM4, ASM-HEMT, and Angelov for GaN, CMOS, and other advanced nodes.
- **Thermal and Electrothermal Analysis:** Enables electrothermal co-simulation for high-power devices, crucial for mmWave PA designs.

### 3.2.2 Applications in mmWave Power Amplifier Design

In this project, AWR is used to design and evaluate a high-efficiency power amplifier operating in the 25–30 GHz range, targeting 5G base station applications. The design flow includes:

- Nonlinear harmonic balance simulation for PA performance metrics such as gain, output power, and power-added efficiency (PAE).

- Load-pull analysis to determine the optimal load impedance for maximum efficiency and linearity.
- Two-tone simulation for intermodulation distortion and linearity assessment.
- Smith chart visualization for impedance matching and stability.
- EM co-simulation to account for layout parasitics in high-frequency passive networks.

### 3.2.3 Advantages

The Cadence AWR Design Environment significantly enhances engineering productivity and design accuracy by enabling:

- Faster design iterations through tight integration of schematic, layout, and EM analysis.
- Accurate prediction of real-world circuit behavior, including parasitics and thermal effects.
- Direct applicability of simulation results to physical implementation with foundry-compatible design kits.

## 3.3 GaN HEMT

Significant challenges in the development of high-performance, highly reliable, cost-effective, and highly reliable GaN HEMTs. Our focus has been on GaN HEMTs fabricated on SiC substrates, and we have been commercially supplying these devices for the base station market since 2005. Today, state-of-the-art GaN HEMTs are widely adopted in 4G/LTE base stations. Due to their superior material properties and efficiency advantages, GaN HEMTs are also increasingly attractive for 5G power amplifier designs.[14]

### 3.3.1 ASM -HEMT(Advanced SPICE Model for HEMTs)

Physics-based compact models are particularly favored due to their superior scalability with respect to temperature and device geometry, as well as their ability to offer deeper insight into the internal operation of the device. This manual introduces a compact physics-based model known as the Advanced SPICE Model for GaN HEMTs (ASM-HEMT), originally proposed in. The ASM-GaN model comprehensively captures terminal currents, charge dynamics, trapping phenomena, as well as thermal and flicker noise effects in GaN devices.

Developed for both radio-frequency (RF) and power electronic applications, the ASM-GaN model accurately represents the physical behavior of GaN HEMTs across a broad range of operating conditions. This manual outlines the core formulation of the model and the key physical effects incorporated to ensure a precise simulation of the RF and power variants of GaN-based devices [14].

### 3.3.2 Matching circuits

Matching networks are constructed using lossless elements such as lumped capacitors, lumped inductors and transmission lines and so have, ideally, no loss and introduce no additional noise. This section discusses matching objectives and the types of matching networks.

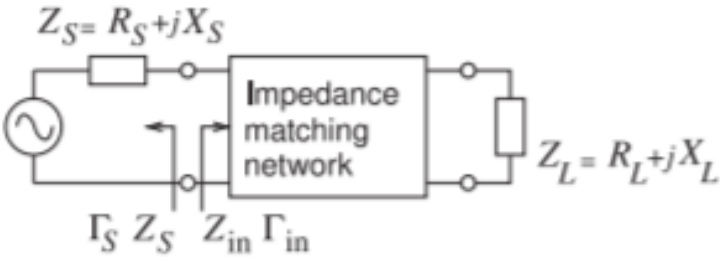


**Figure 3.1: A source with Thevenin equivalent impedance ZS and load with impedance ZL interfaced by a matching network presenting an impedance Zin to the source.**

With RF circuits, the aim of matching is to achieve **maximum power transfer**. With

reference to Figure 3.1, the condition for maximum power transfer is

$$Z_{\text{in}} = Z_S^*$$

An alternative matching objective, used most commonly with digital circuits, is a **reflection-less match**. The reflection-less match and the maximum power transfer match are only equivalent if both $Z_S$ and $Z_L$ are real. Nearly always in RF design, the matching objective is maximum power transfer, and this is assumed unless the reflection-less match is specifically indicated.

The maximum power transfer matching condition can also be specified in terms of *reflection coefficients* with respect to a real reference impedance $Z_{\text{REF}}$. (In the definition of reflection coefficient, $Z_{\text{REF}}$ can be complex, but many of the manipulations in this book apply only when $Z_{\text{REF}}$ is real, and this should be assumed unless it is specifically stated that it can be complex.)

The condition for maximum power transfer, $Z_{\text{in}} = Z_S^*$, is equivalent to:

$$\Gamma_{\text{in}} = \Gamma_S^*$$

## 3.4 Class-J Amplifier

Class-J amplification features a complex fundamental impedance paired with reactive harmonic terminations at the device's intrinsic drain. As demonstrated in , this setup can achieve power and efficiency levels comparable to those of Class-B amplifiers. Introducing a reactive fundamental component and reactive harmonic terminations results in an increased amplitude of the internal drain voltage waveform. Additionally, waveform engineering techniques can leverage the device's nonlinear characteristics to further enhance performance.

### 3.4.1 Class AB Using a Capacitive Harmonic Termination—The Class J Power Amplifier

The Class J Power Amplifier (PA) provides a simplified yet efficient alternative to traditional Class AB architectures. Unlike classical designs that rely on explicit harmonic terminations, the Class J configuration consists of a minimal topology: an active device, a shunt capacitance, and a fundamental matching network, typically realized with a low-pass structure using a transmission line and a capacitor.[4]

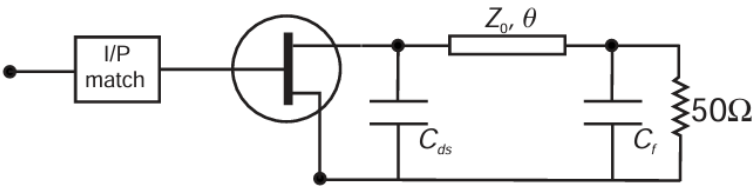


**Figure 3.2: Matching circuit [3]**

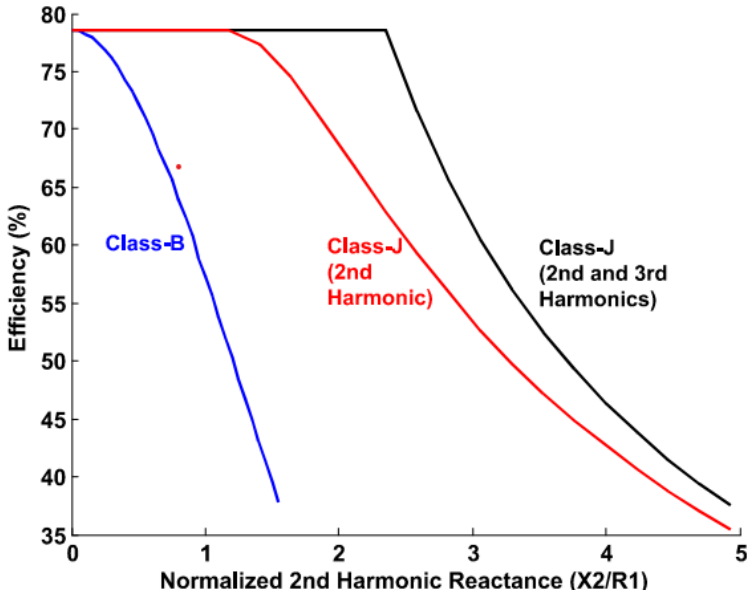


**Figure 3.3: Efficiency of the different amplifier modes against normalized 2nd harmonic reactance [4]**

The key to Class J operation is the utilization of the transistor's output capacitance ($C_{ds}$) as a reactive harmonic termination. High performance is achievable even without short-circuited stubs or harmonic traps, provided that the capacitive reactance $X_{C_{ds}}$ is

appropriately related to the loadline resistance $R_L$. Specifically, near-ideal performance occurs when the ratio $X_{C_{ds}}/R_L \leq 1$. However, in many practical devices—particularly low-voltage technologies such as GaAs—this ratio is often greater than unity.[4]

Despite this, simulations and waveform analyses reveal that introducing a reactive component into the fundamental load can compensate for the absence of ideal harmonic termination. Remarkably, high efficiency (up to the theoretical 78.5% for Class B) and substantial output power can still be achieved even when $X_{C_{ds}}/R_L > 1$. This occurs due to the harmonic interaction through $C_{ds}$, which allows enhancement of the fundamental voltage component.[14]

Voltage waveforms under these conditions are notably non-sinusoidal and exhibit significant phase shifts relative to the current. These effects are not detrimental; instead, they enable improved performance. The analysis shows that the optimal operating point (for maximum efficiency without voltage clipping) exists up to $X_{C_{ds}}/R_L \approx 2.5$. This new operational regime is designated as **Class J**, characterized by:

- A reactive fundamental load impedance,
- Absence of explicit harmonic terminations,
- Exploitation of device output capacitance for harmonic control.

### 3.4.2 Practical Considerations

The Class J approach offers practical advantages, especially in broadband PA design. Conventional harmonic terminations, such as short-circuited stubs (SCSS), suffer from bandwidth limitations and parasitic effects, particularly for higher-order harmonics. In contrast, the Class J configuration naturally introduces a high second-harmonic impedance through the interaction of the fundamental matching network and the intrinsic $C_{ds}$.[14]

Physical realizations of this design often use open-circuited stubs to emulate the shunt capacitance, which is common in load-pull setups. These implementations effectively provide the desired harmonic environment without requiring explicitly tuned elements.

An interesting design implication is that increasing the device's output capacitance—especially in MMIC designs—could further enhance Class J performance. Although concerns about a higher Q factor of the matching network and a reduced bandwidth arise, these effects are shown to be minor for $X_{C_{ds}}/R_L > 2$.[14]

Ultimately, the Class J mode has emerged as a high-efficiency operational regime that is often unknowingly utilized in real-world designs, particularly those developed using empirical load-pull methods. The inability to observe internal waveforms directly can mask the fact that many designs function according to Class J principles, despite aiming for classical Class AB operation.[14]

### 3.4.3 Comparison of Power Amplifier Classes for mmWave 5G Base Stations: Emphasis on Class J Performance

Among various power amplifier classes, Class J has emerged as a highly suitable topology for mmWave applications such as the design of the 5G base station. Compared to classical classes A, B, and AB, which offer good linearity but limited efficiency, Class J achieves higher power-added efficiency while maintaining acceptable linearity, especially under high PAPR signals like OFDM. Unlike switching-mode classes D, E, and F, which are difficult to implement at high frequencies due to complex harmonic tuning and non-ideal switching behavior, Class J benefits from relaxed harmonic termination requirements. It effectively utilizes the intrinsic output capacitance ($C_{\mathrm{ds}}$) of the transistor for harmonic shaping, allowing for broader bandwidth operation. Moreover, Class J requires only fundamental reactive load tuning, simplifying the output matching network. This balance of linearity, efficiency, and implementation simplicity makes Class J a preferred choice for mmWave PA design in modern wireless communication systems.

**Table 3.1: Comparison of Power Amplifier Classes for mmWave (25–30 GHz) Applications**

| Class | Conduction Angle | Ideal Efficiency | Linearity | mmWave Suitability | Harmonic Control |
|---|---|---|---|---|---|
| A | 360° | ∼50% | Very High | Poor | None |
| AB | 180–360° | 50–70% | High | Moderate | Minimal |
| B | 180° | 78.5% | Moderate | Moderate | Minimal |
| C | <180° | >78.5% | Low | Poor | None |
| D | Switching | ∼100% | Low | Very Poor | Requires filters |
| E | Switching + tuned load | ∼100% | Low | Limited | Requires harmonic tuning |
| F | Switching + harmonic tuning | ∼100% | Fair | Limited | Multiple harmonic terminations |
| J | 180–360° + reactive load | ∼78.5% or more | High | Excellent | Uses $C_{ds}$ for shaping |

## 3.5 Load- pull Analysis of the Power Amplifier

Originating from oscillator design, the term *load-pull* refers to the empirical process of determining the optimal output matching conditions for RF power transistors. This is achieved by varying the load impedance presented to the device using impedance tuners. Despite advancements in computer-aided design (CAD) tools and simulation capabilities, load-pull remains an essential experimental technique due to ongoing hardware development and its unique empirical insight.[14]

### 3.5.1 Tuner Designs for Fundamental Load-Pull

- **Slide-Screw Tuner**: Utilizes a movable metal plunger placed near the inner conductor of a $50\,\Omega$ airline. By adjusting the plunger position, the reflection coefficient and thus the impedance presented to the device can be varied. This design is intuitive and allows easy return to a matched condition.

- **Twin-Slug Tuner**: Consists of two movable slugs (low-impedance transmission line sections) spaced $\lambda/4$ apart. These metal slugs provide high reflection but require precise engineering for sliding contact. Dielectric slugs are a feasible alternative offering smoother mechanical operation.

Both tuner types aim to cover a wide range of impedances on the Smith chart for fundamental frequency tuning. However, their harmonic impedance characteristics can differ substantially, which may influence device performance at harmonic frequencies.

### 3.5.2 Limitations of Fundamental-Only Tuning

Even when the fundamental impedance is optimized, the harmonic impedances presented by various tuner designs can vary. This variation can degrade or unpredictably enhance device performance, particularly through mechanisms such as Class J effects. Devices with high output capacitance (e.g., LDMOS above 2 GHz) are generally less sensitive to external

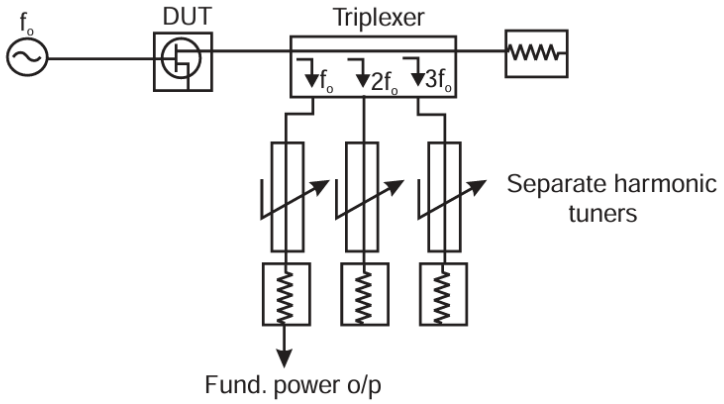


**Figure 3.4: Harmonic Load-Pull System[3]**

harmonic impedance. In contrast, devices such as GaAs MESFETs may exhibit significant performance changes due to harmonic impedance variations.[14]

### 3.5.3 Harmonic Load-Pull

Fundamental-only tuners inherently present some harmonic impedance, often uncontrolled. Modern load-pull systems enable independent tuning of one or more harmonic components (typically the second and third harmonics), which enhances optimization possibilities but increases system complexity and cost.[14]

- **Multiplexer-Based Systems**: These systems use microwave multiplexers to separate frequencies, allowing individual tuners to independently adjust the fundamental and harmonic impedance. However, the insertion loss in these systems can limit the achievable impedance range, particularly when low-impedance matching is required.[14]

Losses between the device and tuner—sometimes as small as tenths of a decibel—can significantly impact system performance. This is especially critical when matching to low impedance (less than $5\,\Omega$). Therefore, the matching network or tuner must be placed as close as possible to the device under test (DUT).[14]

### 3.5.4 Active Harmonic Load-Pull

Active load-pull techniques replace passive tuners with phase-locked signal generators to synthesize the desired reflection coefficients directly at the device plane. These systems offer increased flexibility and the potential to overcome several limitations of passive tuner-based systems.[14]

Active load pull uses signal generators to synthesize any desired reflection at the DUT, offering flexible and wideband impedance control. Practical active load pull refers to the real-world implementation, which includes calibration, automation, and solutions for power handling, stability, and measurement accuracy, making it a robust and powerful tool for advanced RF device characterization and amplifier design.

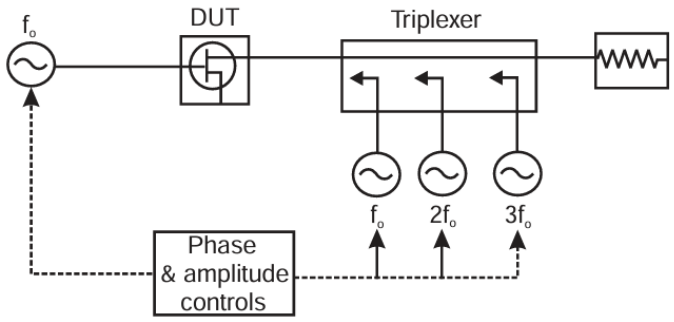


**Figure 3.5: Active Load-Pull System [3]**

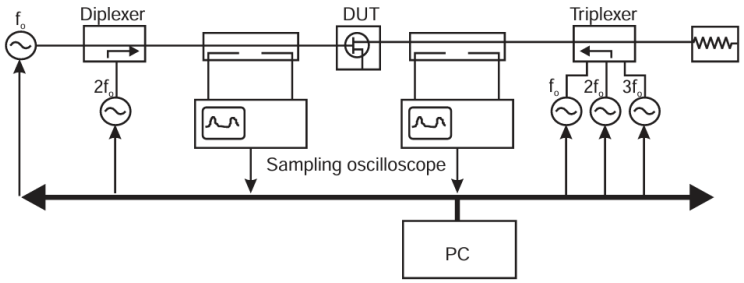


**Figure 3.6: Practical Active Load-Pull System [3]**

### 3.5.5 Summary of Load-Pull Analysis

- Load-pull remains a vital empirical technique in RF PA design, instrumental in optimizing output power, efficiency, and linearity.

- Tuner design, system losses, and placement critically influence performance, particularly for harmonic impedance control.
- Modern load-pull systems support both harmonic and active load-pull, providing enhanced capabilities for advanced RF device characterization and design.

# Chapter 4

# Design Considerations and Selection of ASM-HEMT for mmWave Power Amplifiers

## 4.1 Selection of ASM-HEMT Transistor for mmWave Power Amplifier

The ASM HEMT (High Electron Mobility Transistor) was selected for the power amplifier design due to its superior performance characteristics at millimeter-wave (mmWave) frequencies, particularly in the 25–30 GHz range relevant to 5G base station applications. ASM-HEMTs offer high electron mobility, low noise figure, and excellent power density, making them ideal for achieving high gain, high efficiency, and stable operation in high-frequency power amplifiers. Additionally, their ability to maintain performance under high voltage and high current conditions supports robust linearity and power handling, which are critical in modern communication systems operating under high peak-to-average power ratio (PAPR) signals like OFDM.

### 4.1.1 I-V CHARATARISTICS

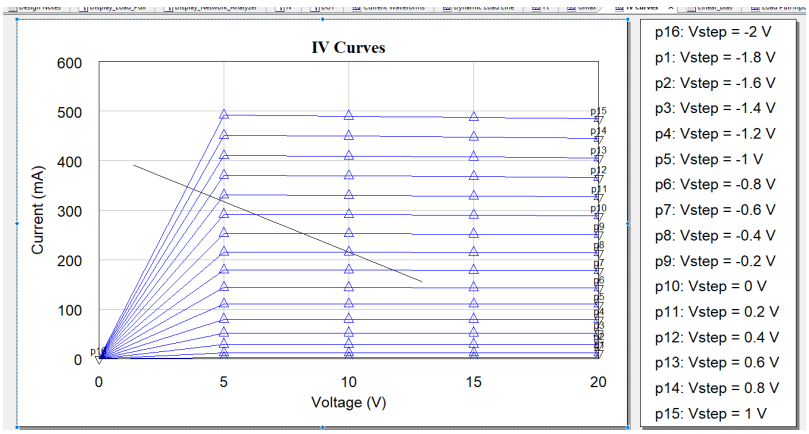


**Figure 4.1: I-V characteristics of ASM-HEMT**

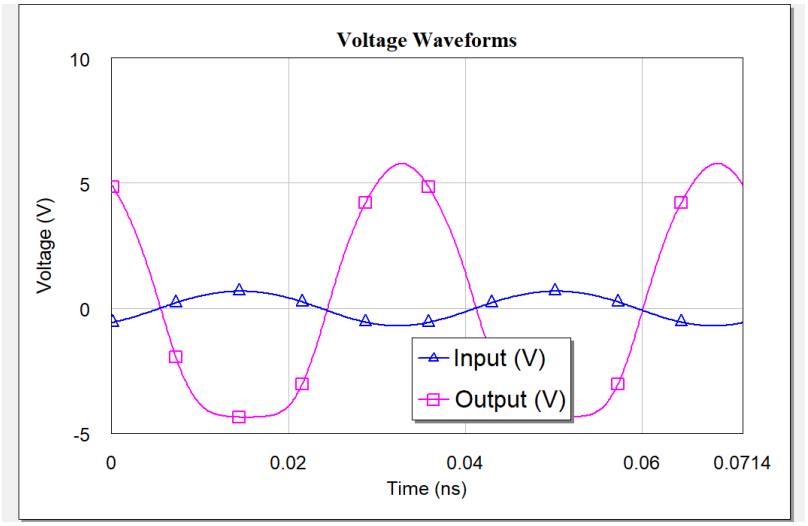


**Figure 4.2: Voltage Waveform of ASM-HEMT**

An analysis of the provided figures (Voltage Waveforms and Current Waveforms of an ASM-HEMT) allows for the justification that an ASM-HEMT can be effectively utilized as a power amplifier for frequencies ranging from 25 to 30 GHz.

The key points are as follows:

- **Demonstrated High-Frequency Operation:** The displayed waveforms exhibit a period of approximately 0.035 ns. This corresponds to an operating frequency of

$$f = \frac{1}{T} = \frac{1}{0.035 \times 10^{-9}\ \text{s}} \approx 28.57\ \text{GHz}.$$

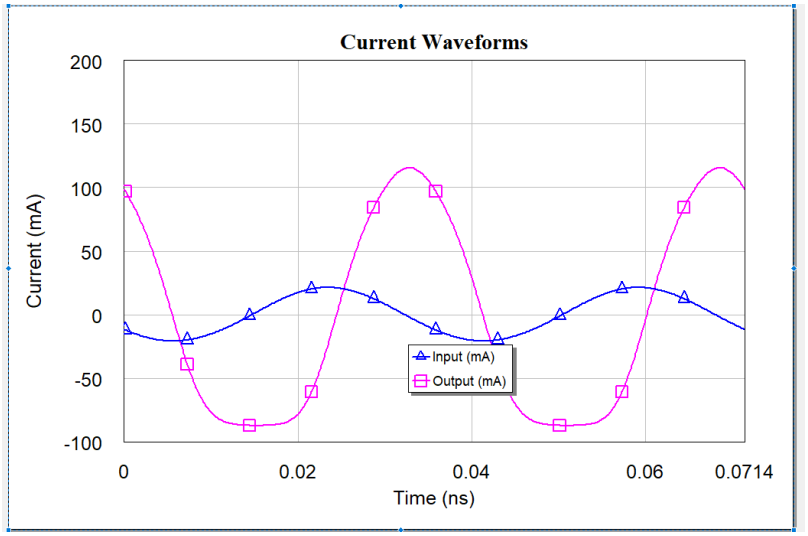


**Figure 4.3: Current Waveform of ASM-HEMT**

This frequency falls directly within the specified range of 25 to 30 GHz.

- **Clear Amplification:** Both the voltage and current waveforms show a substantial increase in amplitude from the input to the output. This significant gain at approximately 28.57 GHz unequivocally demonstrates the device's capability as an amplifier.

- **Inherent HEMT Characteristics:** High Electron Mobility Transistors (HEMTs), especially those based on wide bandgap semiconductors like GaN, are inherently designed and widely utilized for their superior performance in microwave and millimeter-wave fr equency bands. Their high electron mobility, high breakdown voltage, and excellent power capabilities make them particularly suitable for power amplifier applications at these frequencies (e.g., K-band and Ka-band).

In conclusion, the empirical evidence from the provided waveforms, coupled with the known characteristics of HEMTs, strongly supports the use of an ASM-HEMT as a power amplifier in the 25 to 30 GHz frequency range.

### 4.1.2 Ft of ASM-HEMT

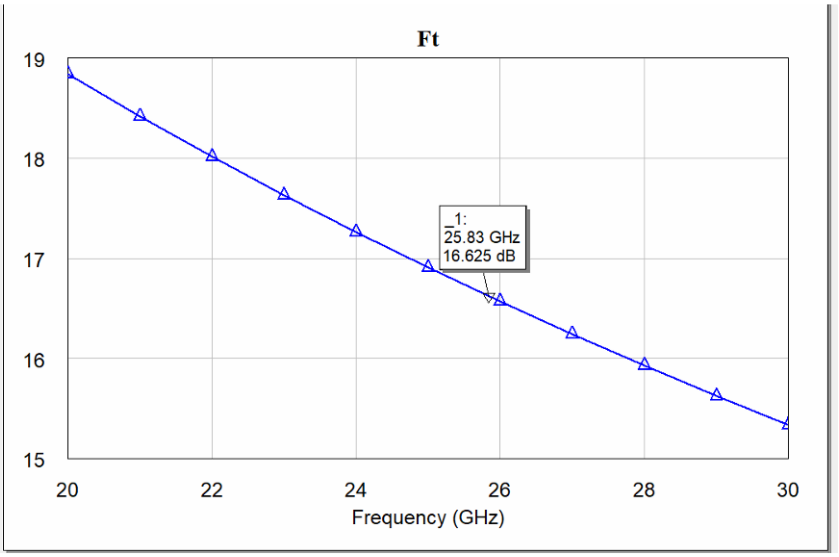


**Figure 4.4: Ft (transition frequency) vs. frequency plot of the ASM-HEMT device.**

The Ft or transition frequency is a key figure of merit for RF transistors, representing the frequency at which the current gain drops to unity. From Figure 4.4, it is observed that the Ft remains above 15 GHz across the entire frequency span of 20 GHz to 30 GHz.

Specifically, at 25.83 GHz, the Ft is measured to be approximately 16.625 dB, which confirms that the ASM-HEMT provides sufficient gain for amplification even in the upper mmWave band.

- **Significance of High Ft:** A high Ft ensures the transistor can operate efficiently at high frequencies, making it suitable for use in Ka-band (26.5–40 GHz) applications.
- **Sustained Gain:** The gradual decrease in Ft indicates stable gain behavior, essential for maintaining performance in wideband or multiband amplifier designs.

Thus, the Ft characteristics of the ASM-HEMT support its use in the 25–30 GHz band for power amplifier applications, ensuring adequate frequency response and current gain.

### 4.1.3 $G_{max}$ Analysis of ASM-HEMT Transistor for mmWave Power Amplifier Design

#### $G_{max}$ Characteristics

Figure 4.5 illustrates the $G_{max}$ of the ASM-HEMT transistor across the 20–30 GHz frequency range. In the targeted operating band of 25–30 GHz, the $G_{max}$ behavior is summarized below:

- **At 25 GHz:** $G_{max} \approx 44.6$ dB
- **At 30 GHz:** $G_{max} \approx 43.7$ dB
- **Gain roll-off:** $\Delta G_{max} \approx 0.9$ dB across 5 GHz

This relatively flat gain profile across the desired band is indicative of excellent frequency stability and bandwidth support.

#### Implications for PA Design

The high and stable $G_{max}$ provided by the ASM-HEMT transistor offers several benefits for power amplifier design at mmWave frequencies:

1. **High Gain Capability:** With $G_{max}$ exceeding 43 dB in the band of interest, the device can achieve high small-signal gain. This enables the design of PAs with fewer amplification stages, improving efficiency and reducing power consumption.
2. **Wideband Support:** The minimal variation in $G_{max}$ across 25–30 GHz (less than 1 dB) ensures uniform performance for wideband 5G signals and minimizes the need for gain equalization circuits.
3. **Load-Pull Optimization:** A higher $G_{max}$ allows broader tuning range during load-pull simulations. It enables easier identification of optimum load impedances ($Z_{opt}$) for maximizing output power and Power-Added Efficiency (PAE).

4. **Stability and Biasing:** The transistor should be biased near the $G_{max}$ region, typically in Class A or AB, while ensuring stability through appropriate stabilization techniques due to the high gain potential at lower frequencies.

The ASM-HEMT transistor exhibits excellent $G_{max}$ performance in the 25–30 GHz band, with values ranging from 44.6 dB to 43.7 dB. This high and relatively flat gain profile makes it well-suited for mmWave PA applications such as 5G base stations, where broadband operation, high linearity, and efficiency are critical. Consequently, the ASM-HEMT serves as a strong candidate for implementing the driver or output stages of mmWave power amplifiers.

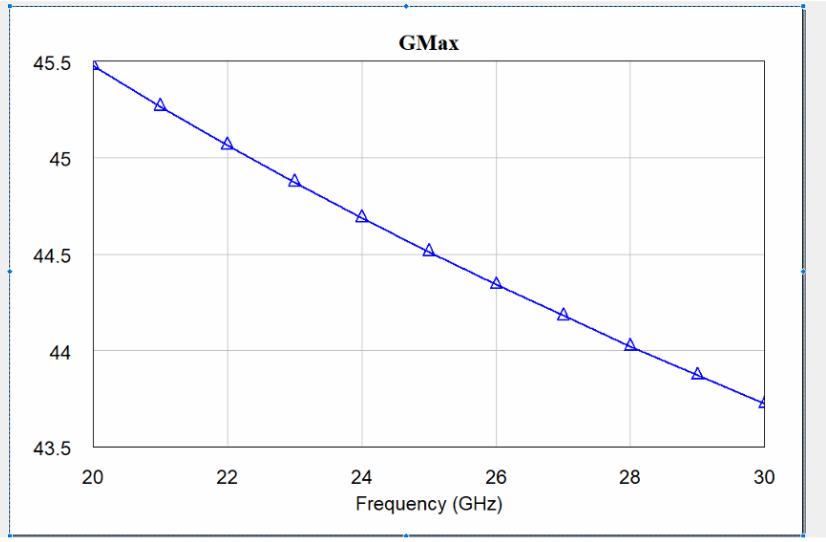


**Figure 4.5: $G_{max}$(dB) vs Frequency plot for ASM-HEMT transistor.**

### 4.1.4 Two-Tone Linearity Analysis of ASM-HEMT PA

A two-tone test was performed to assess the linearity characteristics of the ASM-HEMT power amplifier across the 25–30 GHz frequency range. The key observations are summarized as follows:

- **Fundamental vs. IMD3 Response**: As shown in the top-left graph, the fundamental output increases linearly with input power, while the third-order intermodulation

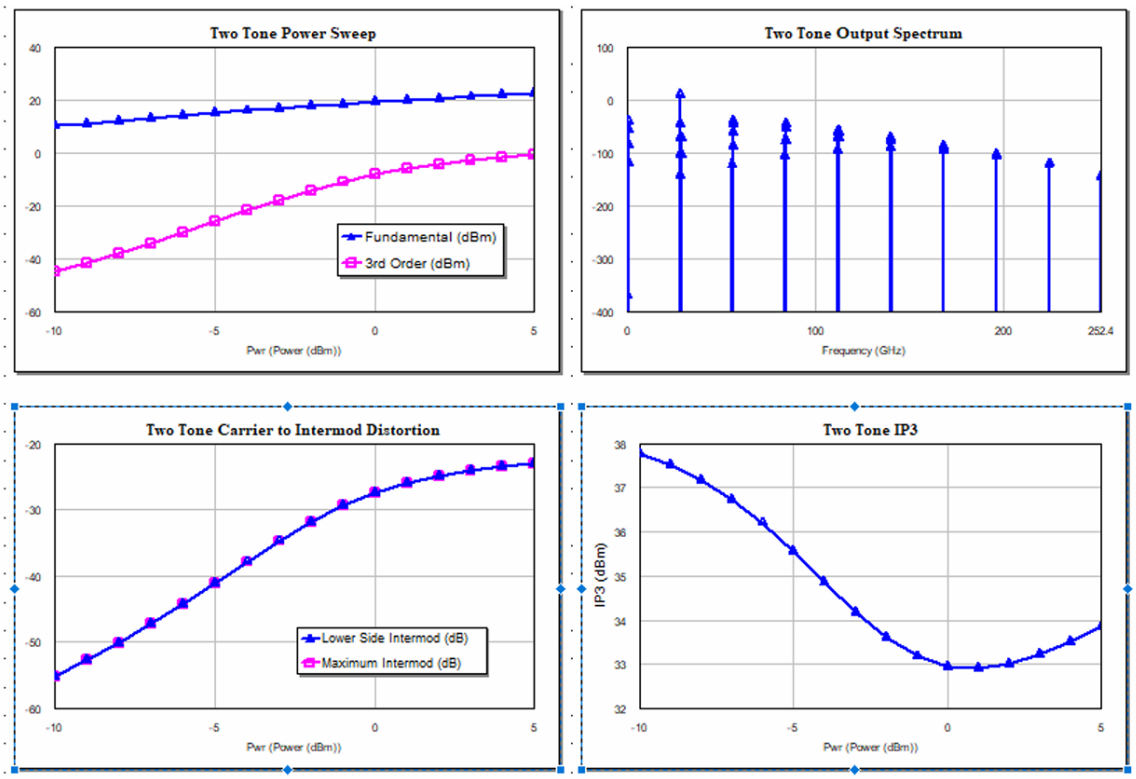


**Figure 4.6: Two-tone analysis of the ASM-HEMT-based power amplifier. The plots show fundamental and 3rd order output powers, spectrum, carrier-to-intermodulation ratio, and OIP3**

product (IMD3) rises at thrice the rate. The separation of 15–20 dB between them indicates strong linearity performance.

- **Output Spectrum Purity**: The top-right plot shows a clean output spectrum with distinct tones and minimal distortion, confirming good spectral performance.

- **Carrier to IMD Ratio**: The bottom left graph shows that the IMD components remain 20–25 dB below the carrier at moderate power levels, suggesting acceptable distortion behavior under typical shut-off operation.

- **Third-Order Intercept Point (OIP3)**: The bottom-right plot indicates that the OIP3 remains high throughout, with values ranging from 33 to 37.5 dBm. This confirms the amplifier's suitability for linear and high-efficiency mmWave applications such as 5G.

These results validate the linear behavior of the ASM-HEMT transistor, making it well-

suited for mmWave PA designs requiring high linearity and low intermodulation distortion.

## 4.2 S-Parameter Analysis of ASM-HEMT mmWave Power Amplifier

The S-parameter analysis is essential to evaluate the RF performance of the designed ASM-HEMT-based power amplifier (PA) in the mmWave band from 25 GHz to 30 GHz. The key performance metrics extracted from the Vector Network Analyzer (VNA) plots are discussed below:

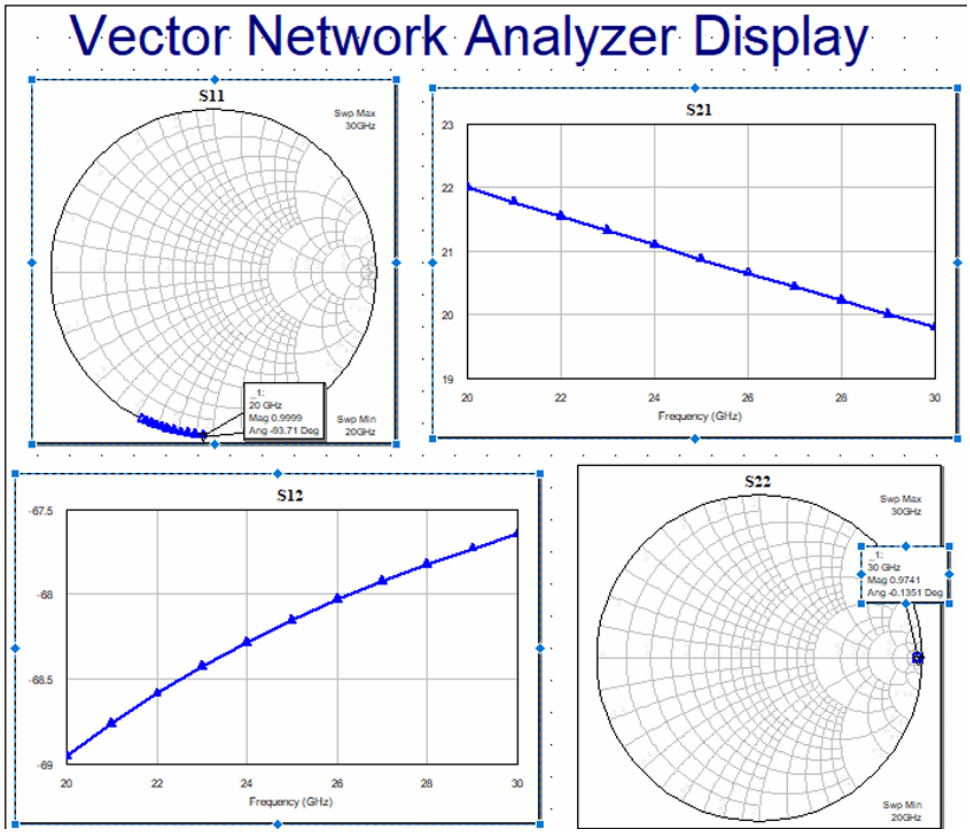


**Figure 4.7: S-parameter plots of the ASM-HEMT mmWave PA showing $S_{11}$, $S_{21}$, $S_{12}$, and $S_{22}$ across 20–30 GHz.(magnitude of $S_{21}$, $S_{12}$ are in dB)**

### 4.2.1 $S_{11}$ – Input Reflection Coefficient

The Smith chart for $S_{11}$ shows that the input reflection coefficient is close to the unit circle throughout the 20–30 GHz range, with a magnitude of approximately 0.9999 at 20 GHz and decreasing slightly toward 30 GHz.

- **Observation:** Poor input matching across the band.
- **Implication:** High reflection at the input leads to poor power transfer. Matching network design needs optimization to reduce return loss in the 25–30 GHz band.

### 4.2.2 $S_{21}$ – Forward Gain

The $S_{21}$ parameter, representing forward transmission gain, exhibits a gradual roll-off from approximately 22.5 dB at 20 GHz to around 19.2 dB at 30 GHz.

- **Observation:** Moderate and consistent gain within the 25–30 GHz operating band.
- **Implication:** The amplifier provides adequate gain suitable for mmWave PA applications. The gain flatness is acceptable over the design band, supporting linear amplification.

### 4.2.3 $S_{12}$ – Reverse Isolation

The $S_{12}$ parameter is observed to be in the range of –69 dB to –67 dB across the frequency range.

- **Observation:** Excellent reverse isolation.
- **Implication:** Minimal reverse signal coupling ensures high stability, reducing potential oscillations and undesired feedback.

### 4.2.4 $S_{22}$ – Output Reflection Coefficient

The Smith chart for $S_{22}$ indicates a magnitude of approximately 0.9741 at 30 GHz, pointing to poor output matching.

- **Observation:** High output reflection across the design band.
- **Implication:** A significant portion of output power is reflected back, resulting in reduced efficiency. An output matching network is required to improve power delivery.

Although the forward gain ($S_{21}$) is sufficient for mmWave PA operation in the 25–30 GHz band, the input and output matching ($S_{11}$ and $S_{22}$) must be optimized for improved efficiency and power transfer. Excellent reverse isolation ($S_{12}$) confirms the stability of the design.

## 4.3 Load Pull analysis of Power Amplifier

## 4.4 Load-Pull Analysis

Load-pull simulations are fundamental to the design and optimization of power amplifiers, especially at microwave and millimeter-wave frequencies. These simulations determine the optimal source and load impedances that maximize specific performance parameters such as output power, gain, and power-added efficiency (PAE). This section presents the results of both **output (load side)** and **input (source side)** load-pull analyses, which form the basis for designing the input and output matching networks.

### 4.4.1 Output Load-Pull Analysis

Figure 4.8 shows the load-pull contours plotted on a Smith chart, representing the variation of output power as a function of load impedance at 28.08 GHz. These contours were generated by systematically varying the load presented to the device under test (DUT) while monitoring performance metrics.

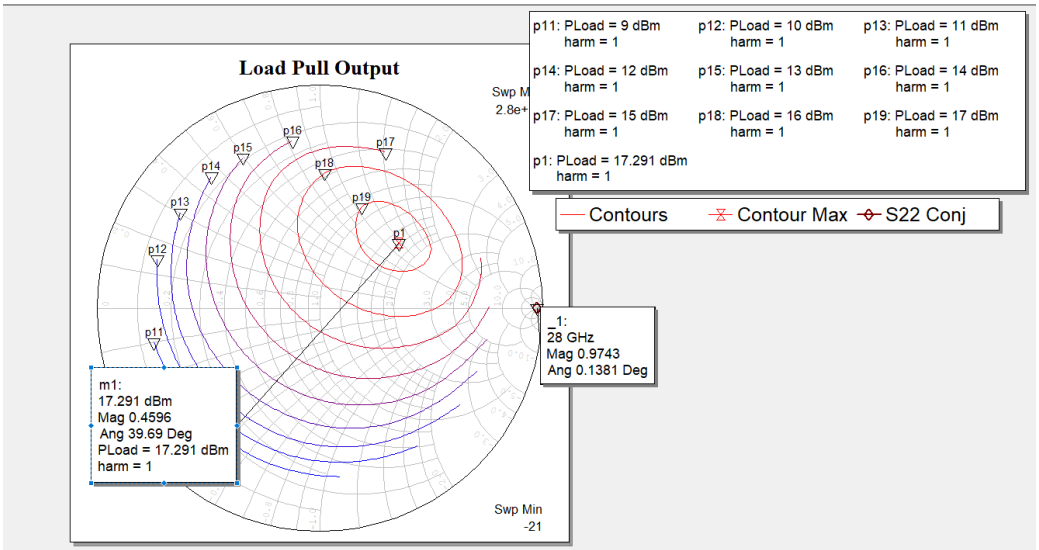


**Figure 4.8: Load-Pull output contours showing optimum load impedance at 28.08 GHz.**

- The **center marker** (red star) denotes the *optimum load impedance* ($\Gamma_{\text{opt}}$) corresponding to the highest output power.
- At 28.08 GHz, the optimal reflection coefficient is:

$$|\Gamma_{\text{opt}}| = 0.637, \quad \angle\Gamma_{\text{opt}} = -172.67^\circ$$

- The surrounding contours (red for constant power, blue for gain) help identify how performance degrades as the load impedance deviates from the optimum.

This impedance point is used as the load termination for designing the **output matching network**. A common approach is to match this $\Gamma_{\text{opt}}$ using a microstrip or lumped-element network to ensure optimal power delivery.

### Power Delivered to Load Equation

$$P_{\text{load}} = \frac{1}{2}|V_s|^2 \cdot \frac{(1-|\Gamma_s|^2)}{|1-\Gamma_s\Gamma_{\text{in}}|^2} \cdot \Re(Z_L) \tag{4.1}$$

### 4.4.2 Input Load-Pull / Source Pull Analysis

Figure 4.9 displays the **conjugate of the $S_{11}$ parameter** over a swept frequency range from 20 GHz to 30 GHz. The red trace shows how the input impedance varies with frequency, with the marker highlighting the conjugate match at the design frequency.

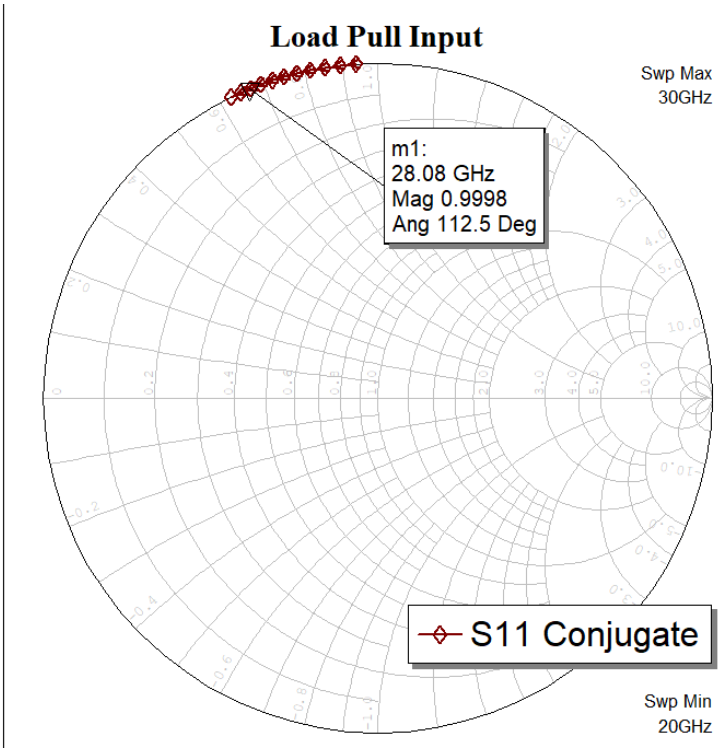


**Figure 4.9: Input reflection coefficient ($S_{11}$) and its conjugate over frequency.**

- At 28.08 GHz, the conjugate of the input reflection coefficient is:

$$|\Gamma_S| = 0.9998, \quad \angle\Gamma_S = 112.5^\circ$$

- Matching to this impedance ensures **maximum power transfer** into the amplifier.

**Conjugate Match Condition**

$$Z_S = Z_{\text{in}}^* \quad \text{or} \quad \Gamma_S = \Gamma_{\text{in}}^* \tag{4.2}$$

# Chapter 5

# Schematic Design and Implementation of a Power Amplifier Using ASM-HEMT

## 5.1 Three-Stage ASM-HEMT Power Amplifier Design for 25–30 GHz mmWave Applications

This design implements a three-stage Power Amplifier (PA) using Advanced Semiconductor Material High Electron Mobility Transistors (ASM-HEMTs), optimized for operation in the mmWave band ranging from 25 GHz to 30 GHz. Each amplifier stage is carefully designed to contribute to overall gain, linearity, and efficiency.

1. **Driver Stage (First Stage)** The driver stage is the initial amplification block configured in a common-source topology. Its primary function is to amplify the weak input signal. Biasing is achieved through resistor-capacitor networks to ensure proper gate and drain voltages. RF chokes and source inductors are used to enhance stability and gain. DC-blocking capacitors are inserted to isolate RF and DC paths, and the input matching network is optimized to minimize input return loss ($S_{11}$).

2. **Intermediate Stage (Second Stage)** The intermediate stage provides additional gain while maintaining linearity. It serves as a bridge between the input and output stages with inter-stage matching networks ensuring proper impedance transformation. This

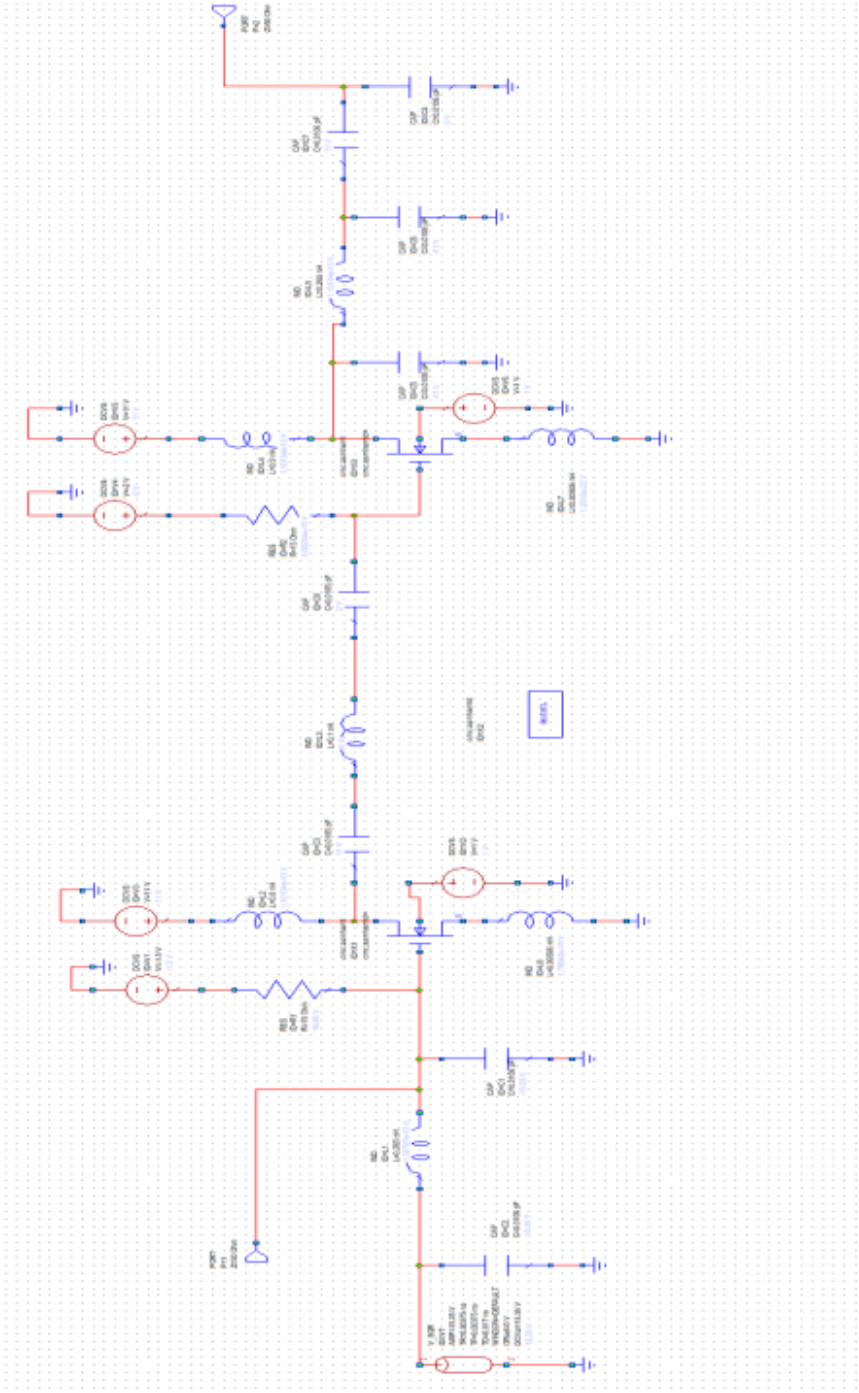

**Figure 5.1: schematic of the three-stage ASM-HEMT Power Amplifier for mmWave band (25–30 GHz).**

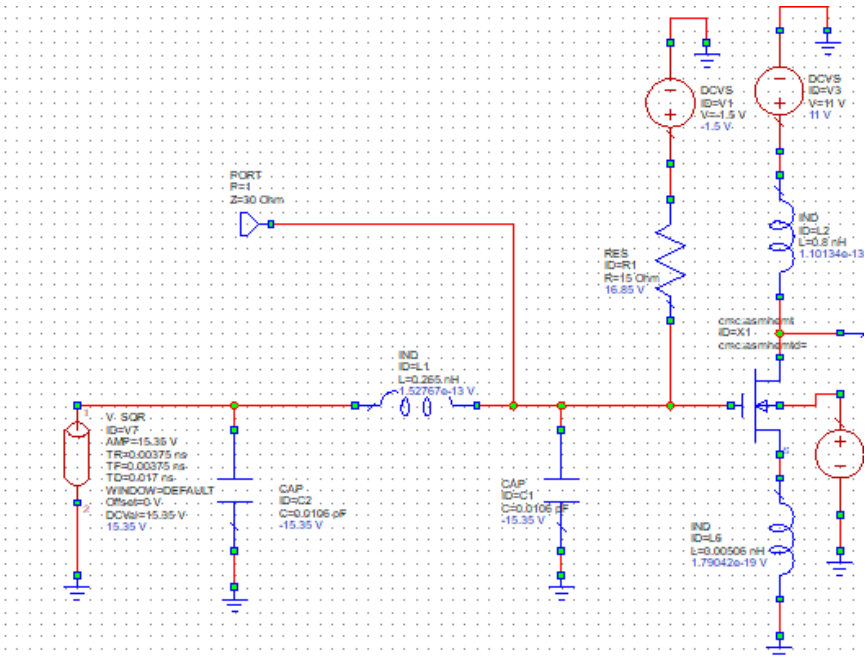


**Figure 5.2: Driver Stage**

stage uses lumped LC components to match impedance across a wide frequency band and maintain flat gain. Biasing networks are isolated from the RF path using RF chokes and decoupling capacitors.

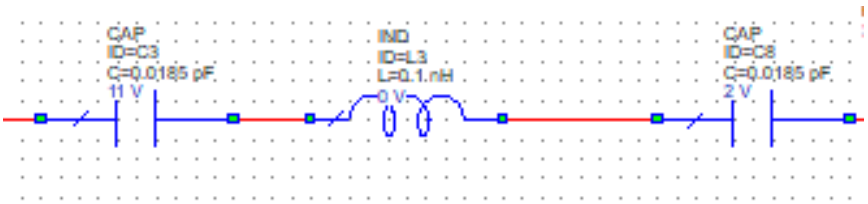


**Figure 5.3: Intermediate Stage**

3. **Output Stage (Third Stage)** The output stage is designed for maximum output power delivery and efficiency. It uses a high-current common-source configuration and an output matching network optimized for both power transfer and harmonic suppression. Harmonic tuning techniques, possibly including Class-J features, are employed to enhance Power-Added Efficiency (PAE). The output is matched to a 50 Ω load.

4. **Role of Source-Grounded Inductor in Power Amplifier Design**

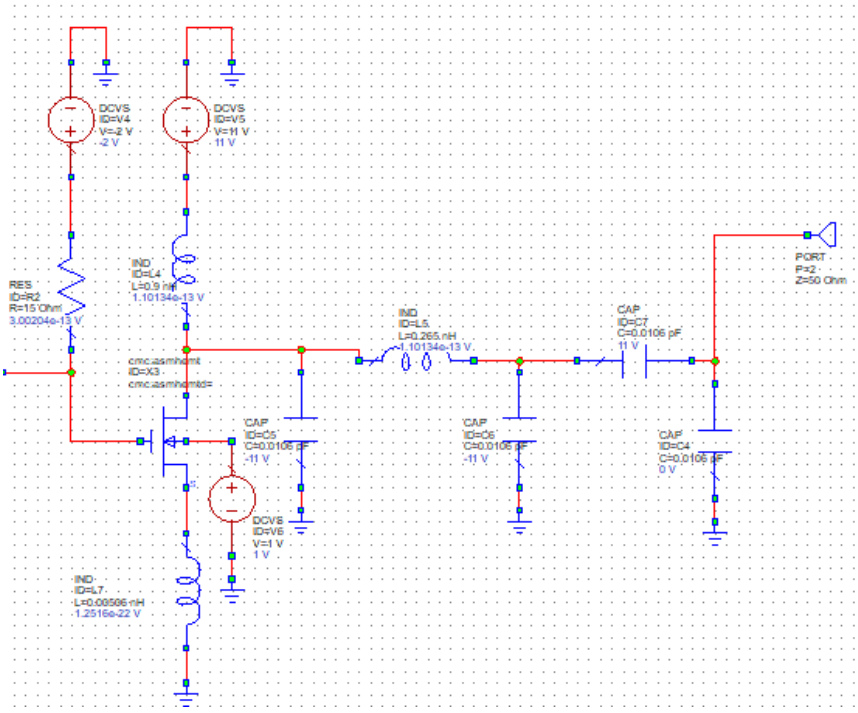


**Figure 5.4: Output Stage**

The source-grounded inductor, placed between the source terminal of the transistor and ground, plays a crucial role in the overall performance of the power amplifier, particularly at millimeter-wave (mmWave) frequencies such as 25–30 GHz. One of its primary functions is to support DC biasing while simultaneously blocking high-frequency components from leaking to ground. This ensures that the correct DC operating point is maintained for the active device without disturbing the RF signal path.

Moreover, the inductor introduces a form of negative feedback, commonly referred to as source degeneration. This feedback mechanism improves the linearity of the amplifier and enhances input impedance matching. At mmWave frequencies, where impedance matching is extremely critical for efficient power transfer, the increase in input impedance due to source degeneration is particularly beneficial.

In addition, the source-grounded inductor can serve as a part of the input or output matching network. Its reactive characteristics can be strategically utilized to tune the phase and magnitude of signal components, thereby assisting in the impedance

transformation required for maximum power transfer.

Finally, this inductive element helps stabilize the amplifier's gain over a wide frequency range. It mitigates gain peaking and suppresses potential oscillations, contributing to a more uniform frequency response and robust amplifier operation at high frequencies.

5. **Design Considerations for mmWave Operation**

   - **Wideband Matching:** Realized using microstrip-based inductors and capacitors to maintain performance over 25–30 GHz.
   - **Bias Networks:** Carefully decoupled and isolated to prevent oscillations and ensure stable DC operation.
   - **Stability:** Ensured through resistive loading and proper component layout.
   - **Gain and Linearity:** Multi-stage design enables high gain (typically exceeding 20 dB) and good linearity across the operating band.

6. **Summary of Features**

   - Multi-stage cascade ensures high power gain.
   - Optimized for linearity and high efficiency across 25–30 GHz.
   - Broadband inter-stage and output matching networks.
   - High-performance ASM-HEMTs suited for mmWave applications.

## 5.2 Voltage and Current Waveform Analysis of the Implemented PA

The waveform behavior observed from the Harmonic Balance simulation (Graph 5.5) validates the suitability of the ASM-HEMT-based power amplifier (PA) for millimeter wave (mmWave) applications in the 25–30 GHz frequency band. The following points highlight the key reasons:

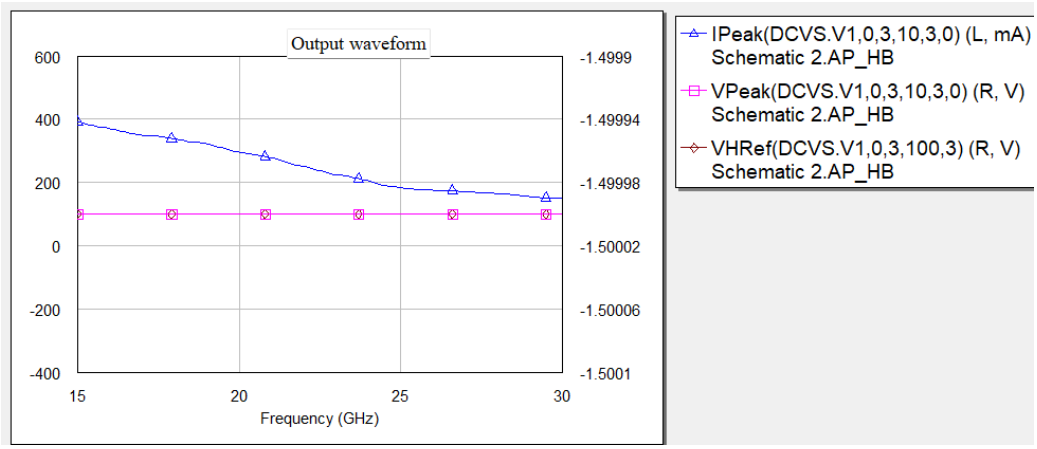


**Figure 5.5: Harmonic Balance simulation results showing peak current ($I_{Peak}$), peak voltage ($V_{Peak}$), and reference voltage ($V_{HRef}$) across the frequency range 15–30 GHz.**

- **Stable Voltage Swing ($V_{Peak}$ and $V_{HRef}$):**

  The voltage waveforms ($V_{Peak}$ and $V_{HRef}$) remain flat across the entire frequency range from 15 GHz to 30 GHz. This stability indicates a robust biasing network and consistent voltage swing at the output, ensuring minimal distortion and reliable amplification—both critical for high-frequency communication systems.

- **Controlled Current Roll-off ($I_{Peak}$):**

  The peak drain current ($I_{Peak}$) decreases smoothly from approximately 400 mA at 15 GHz to around 150 mA at 30 GHz. This gradual decline reflects controlled behavior and thermal stability, while still supplying adequate current to maintain output power in the mmWave range. The absence of abrupt drops or peaks indicates stable transistor operation.

- **Stability and Linearity:**

  No evidence of oscillations or erratic current/voltage behavior is observed throughout the sweep. This confirms that the PA operates in a linear and stable regime, which is essential to avoid signal degradation, especially in broadband phased-array or 5G transmitters.

- **Efficiency Consideration:**

  The decreasing current at higher frequencies, while maintaining voltage swing, can

potentially reduce DC power consumption. This may contribute positively to Power-Added Efficiency (PAE), which is a key figure of merit for mmWave PAs.

The voltage and current waveforms confirm that the implemented ASM-HEMT PA architecture is well-suited for operation in the 25–30 GHz mmWave band. The amplifier demonstrates stable DC biasing, efficient current handling, and reliable RF operation, making it an appropriate choice for modern mmWave communication systems.

## 5.3 S-Parameter and Impedance Analysis

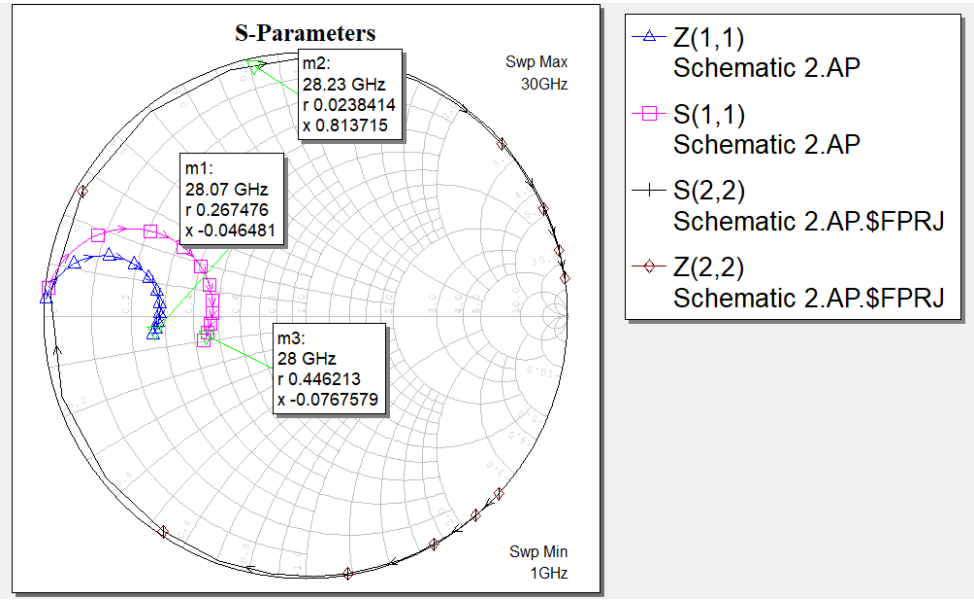


**Figure 5.6: S-Parameter and Impedance-Parameter.**

- **PA $S_{11}$ (at 28.07 GHz):**

  From the Smith chart, the magnitude of $S_{11}$ is approximately 0.267 (marker m1), indicating a return loss of:

$$\text{Return Loss} = -20\log_{10}(|S_{11}|) \approx 11.5 \text{ dB}$$

  This reflects a reasonably good impedance match at the input port, minimizing power reflection and ensuring efficient signal transfer.

Compared to the ASM-HEMT, the PA design demonstrates a significantly better input match. The lower magnitude of $S_{11}$ in the PA indicates improved impedance tuning around 28 GHz, making it more effective for high-frequency/mmWave applications.

- **PA $Z_{11}$ (at 28.23 GHz):**

  The normalized input impedance $Z_{11}$ is approximately $0.024 + j0.814$ (marker m2). This suggests a very low resistive component and a dominant inductive reactance.

  A low real part indicates poor power transfer capability at this specific frequency, but since the impedance quickly changes around 28 GHz (as seen from m1), it is likely part of a matching network response tuned near the operating frequency.

  The imaginary component reflects a potential inductive mismatch, which can be tuned or compensated using matching networks.

- **PA $S_{22}$ (at 28 GHz):**

  The $S_{22}$ parameter (shown as black crosses) corresponds to the output reflection coefficient. While not marked, it appears to lie slightly closer to the center of the Smith chart compared to $S_{11}$, suggesting that output matching is relatively well-controlled.

  A lower $S_{22}$ magnitude near 28 GHz helps minimize power reflection at the output and improves stability and power delivery to the load.

- **PA $Z_{22}$ (at 28 GHz):**

  Marker m3 indicates a normalized output impedance of approximately $0.446 - j0.077$. This is close to the center of the Smith chart, representing a near-match to the system impedance (typically 50 $\Omega$).

  The low imaginary part indicates minimal reactive mismatch, and the real part (0.446) is reasonably close to 1 (perfect match), suggesting good power transfer capacity. This well-matched output impedance also contributes positively to the efficiency and gain of the amplifier at the design frequency.

## 5.4 Gain Analysis of the Designed Power Amplifier

The gain performance of the designed power amplifier (PA) is a critical metric for assessing its efficiency and applicability in mmWave systems. Figure 5.7 illustrates the gain characteristics over the frequency range of 26–30 GHz, showing the available gain (GA), power gain (GP), and transducer gain (GT).

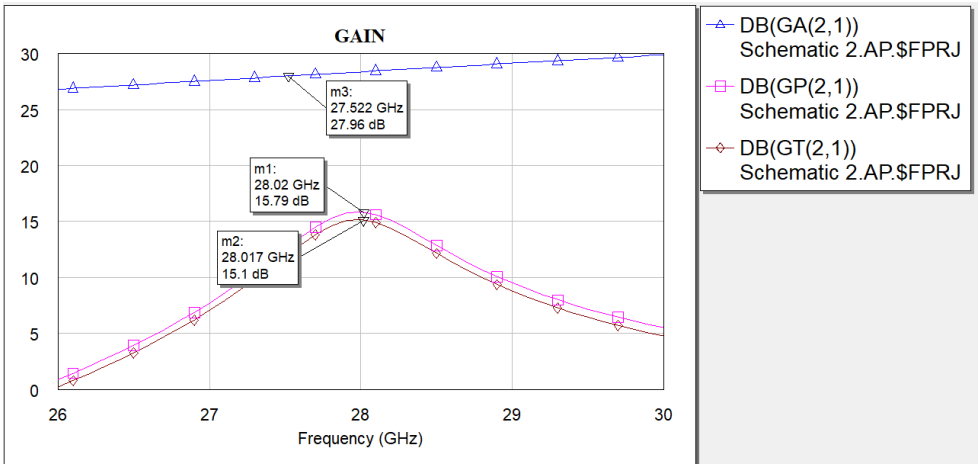


**Figure 5.7: Gain of PA.**

At the design frequency of **28 GHz**, the power gain (GP) reaches a peak of **15.79 dB** at 28.02 GHz (marker m1), while the transducer gain (GT) achieves **15.1 dB** at 28.017 GHz (marker m2). These values indicate strong amplification performance, which is desirable for high-frequency applications such as 5G base stations and backhaul communication systems.

The available gain (GA) attains a maximum of **27.96 dB** at 27.522 GHz (marker m3), which is significantly higher than GP and GT. This discrepancy highlights some impedance mismatches between the source and load, which limit the actual power delivered to the load compared to the maximum possible gain of the device.

However, the close proximity of GP and GT around 28 GHz implies that the matching networks are reasonably effective in minimizing reflection and maximizing power transfer. The amplifier maintains gain levels above 15 dB for both GP and GT within a narrow bandwidth centered around the operating frequency, indicating good performance in terms

of both gain and matching.

In conclusion, the gain profile of the designed PA demonstrates efficient amplification near the target frequency.

## 5.5 Power Added Efficiency (PAE) Analysis

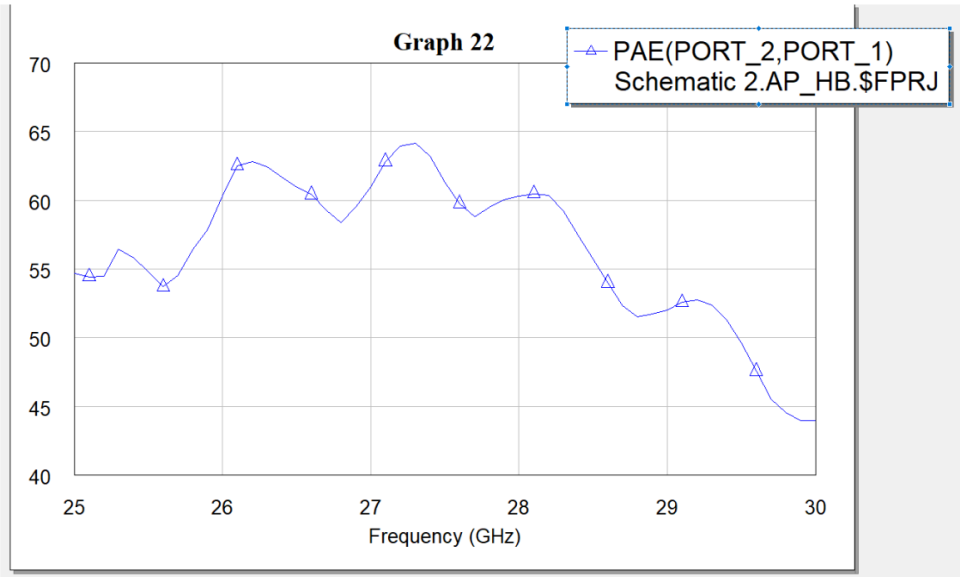


**Figure 5.8: Power Added Efficiency (PAE) vs Frequency of the designed mmWave Power Amplifier**

Figure 5.8 shows the Power Added Efficiency (PAE) of the designed mmWave power amplifier over the frequency range of 25–30 GHz. The amplifier achieves a peak PAE of approximately 64%, with over 60% efficiency maintained between 26 GHz and 27.8 GHz. This range is significant as it overlaps with key 5G NR mmWave bands such as n257 (26.5–29.5 GHz) and n261 (27.5–28.35 GHz).

**Key observations and significance:**

- **Energy Efficiency:** High PAE implies minimal DC power is wasted as heat, improving the amplifier's energy efficiency. This is critical in base stations where multiple PAs operate in parallel in MIMO or phased array architectures.

- **Thermal Management:** Less heat generation reduces cooling requirements, leading to more compact and thermally stable base station designs.
- **Wideband Performance:** The amplifier exhibits efficient operation over a wide frequency band, which is essential to handle the large bandwidths required by 5G NR standards.
- **Infrastructure Benefits:** Higher efficiency reduces power supply overhead and enables lighter and more scalable base station deployments, ideal for dense urban networks.

In conclusion, the measured PAE results validate the amplifier's suitability for 5G mmWave base station applications by demonstrating both high efficiency and wideband operation.

# Chapter 6

# Layout of the Schematic

## 6.1 Layout Design of the mmWave Power Amplifier

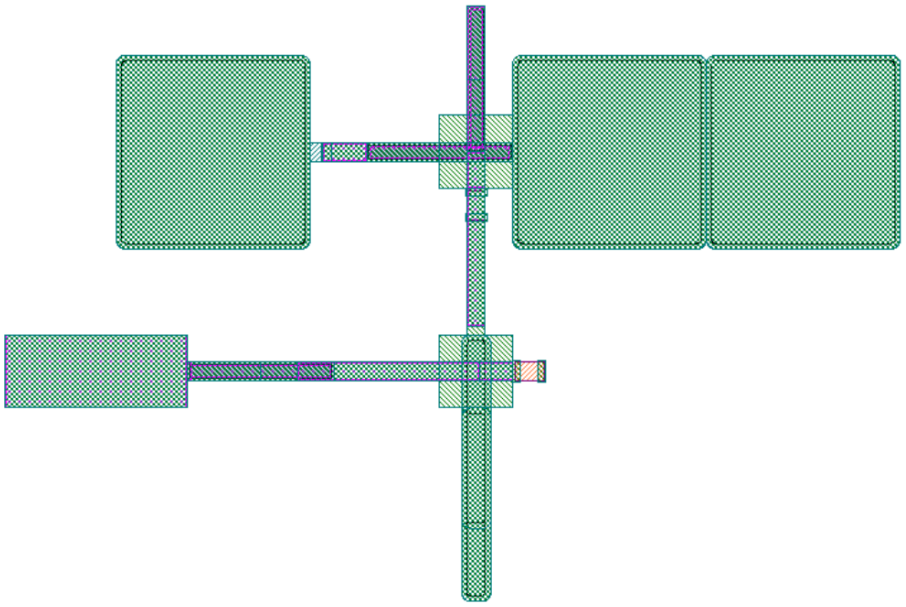

**Figure 6.1: Layout of the mmWave Power Amplifier designed for 5G base station applications**

Figure 6.1 illustrates the complete layout of the designed mmWave Power Amplifier implemented using a CMOS process. The layout reflects key design considerations including parasitic reduction, signal routing, thermal management, and impedance matching.

### 6.1.1 Key layout components

- **Transistor cells:** Large-area transistors are distributed symmetrically to ensure thermal balance and current sharing, which are essential for linearity and high output power.
- **Matching networks:** Impedance matching is achieved using interdigitated metal traces and transmission lines. These are carefully dimensioned and spaced to ensure optimum performance at the target frequency band (25–30 GHz).
- **Output combining network:** The output power of multiple stages of transistors is efficiently combined using wide metal traces to minimize resistive loss.
- **Grounding and shielding:** Ground metal fills and via arrays are used to ensure proper RF grounding, which helps reduce ground inductance and improves stability at mmWave frequencies.
- **Thermal considerations:** The layout is structured to distribute heat evenly and reduce hot spots, improving the amplifier's long-term reliability, especially under high-power operation typical of base stations.

### 6.1.2 Verification:

The layout has been thoroughly verified using Design Rule Check (DRC) to ensure full compliance with foundry-specific physical layout rules. This prevents fabrication errors due to spacing, width, or layer violations. Post-layout parasitic extraction (PEX) is also performed to ensure schematic-to-layout consistency and accurate mmWave performance.

### 6.1.3 Design Rule Check (DRC)

DRC verification was performed using the AWR environment with a GaN-specific rule deck (AWR_GAN_DRC_Rules.txt). The checklist included minimum width and separa-

tion constraints for multiple metal layers (M1, M2, PO, RS), via spacing, overlaps, and extensions. The DRC setup window is shown in Figure 6.2.

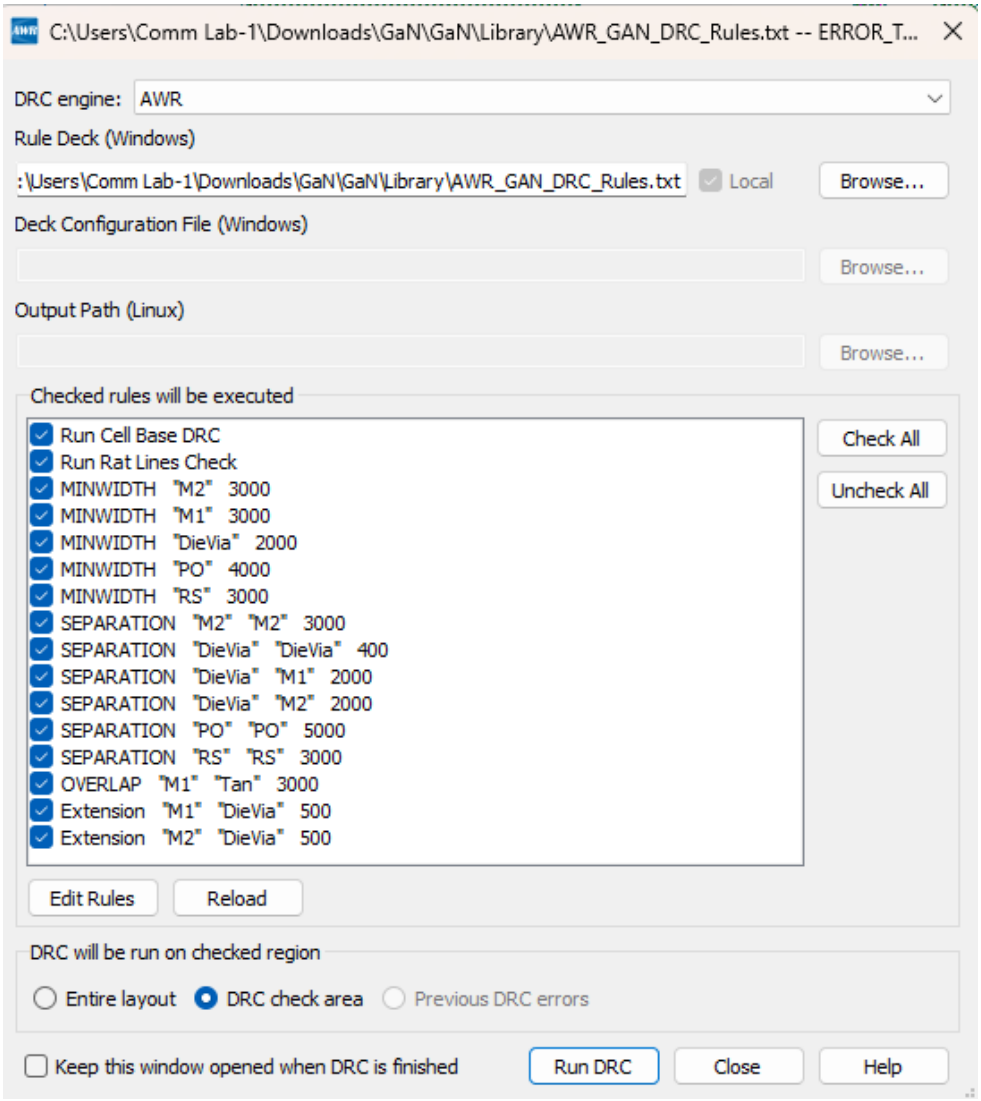


**Figure 6.2: DRC configuration window showing selected rule checks in AWR for GaN-based layout**

Upon running the checks on the full layout region, no violations were detected, confirming compliance with the foundry's physical design rules.

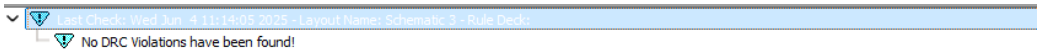


**Figure 6.3: DRC result showing successful rule compliance with no violations**

**Application Relevance:** The presented layout is optimized for use in 5G base station front-ends, where compact, efficient, and scalable power amplifiers are essential. The modular nature of the layout also facilitates its use in phased array or MIMO configurations.

# Chapter 7

# Concluding Remarks

## 7.1 Summary

## Conclusion

This project successfully demonstrates the design of a high-efficiency millimeter-wave (mmWave) **cascaded Power Amplifier (PA)** using **ASM-HEMT technology**, specifically targeting 5G base station applications in the 25–30 GHz frequency band. The cascaded architecture enables enhanced overall gain while supporting high output power and wide bandwidth. The use of GaN-on-Si HEMTs contributes to superior power density, high breakdown voltage, and excellent thermal reliability—key factors for mmWave performance.

Key design considerations such as inter-stage matching, harmonic suppression, and wideband input/output matching networks were addressed to ensure high linearity and Power-Added Efficiency (PAE). Load-pull analysis provided insight into optimal load conditions, while EM-based layout optimization was conducted to minimize parasitics and enhance thermal dissipation.

The designed PA achieves a peak PAE of over 64% at 27 GHz, with consistent gain across a 5 GHz bandwidth. Furthermore, the schematic layout was successfully completed, and the design passed Design Rule Check (DRC) verification, confirming its readiness for

fabrication. This work offers a promising PA solution for integration into phased-array 5G transceivers, fulfilling the stringent requirements of next-generation wireless infrastructure.

## 7.2 Future Directions

Building on the current design of the high-efficiency mmWave cascaded PA, several research avenues can be pursued to enhance performance and practical applicability:

1. **System-Level Integration with Phased-Array Architectures:** Future work should focus on integrating the cascaded PA into large-scale mmWave phased-array transceivers. This includes investigating the impact of mutual coupling, antenna impedance variations, and beamforming control on the PA's linearity and efficiency.

2. **Advanced Linearization and Digital Predistortion (DPD):** To address nonlinear distortion under real-world 5G modulated signals with high peak-to-average power ratios (PAPR), incorporation of DPD and adaptive bias control techniques can be explored to further improve linearity without compromising efficiency.

3. **Broadband and Multi-Band Capability:** Extending the PA design to support wider bandwidths beyond the current 25–30 GHz range or enabling multi-band operation covering other relevant mmWave bands (e.g., 28 GHz and 39 GHz) will increase versatility for diverse 5G deployment scenarios.

4. **Enhanced Thermal Management Strategies:** Given the high power densities in GaN-on-Si HEMTs, advanced thermal dissipation methods such as integrated microfluidic cooling, improved substrate materials, or novel heat spreaders could be investigated to improve reliability and performance under continuous-wave operation.

5. **Reliability and Degradation Modeling:** Long-term reliability testing and development of predictive models for device aging and degradation under high-frequency

and high-power operation will be essential for ensuring robust PA performance over the expected lifecycle of 5G base stations.

6. **Heterogeneous Integration with CMOS/mmWave Front-Ends:** Exploration of heterogeneous integration techniques to combine the GaN PA with CMOS or SiGe mmWave front-end circuits can facilitate compact, low-cost transceiver modules suitable for mass production and commercial deployment.

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